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(6) STUDY OF ELECTRONIC TRANSPORT AND BREAKDOWN IN THIN INSULATING FILMS.

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Recent progress is reported in an ongoing program of studies of high-field effects in thin insulating films on semiconducting substrates. The investigations reported here include further studies of the high-field generation of interface states in the Si-SiO_2 system, description of a method for measuring interface state densities at low temperatures, a preliminary report of Auger observations of interface states in the Si-SiO_2 system, and the results of further studies of high-field effects in the metal-aluminum oxide-silicon system.

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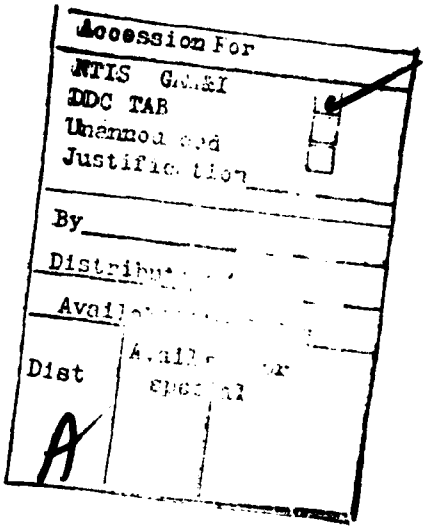


1. INTRODUCTION

We report here on recent progress in an ongoing program of research which is directed toward a basic understanding of the electronic properties of thin insulating films and of the interfaces of such films with semiconductors and metals. Of particular interest are the high-field properties, including charge-carrier injection through the interfaces, electronic transport through the insulator, charge-carrier trapping and recombination at the interfaces and in the insulator, the high-field generation of interface states and trapping centers, and the mechanisms leading to dielectric breakdown. High-field phenomena relevant to very large-scale integration are of especial interest. An objective of the program is to provide a rational basis for the choice of materials, processing methods and treatment of the insulating films and structures to obtain the desired performance and reliability. The insulating films under study at the present time are silicon dioxide and aluminum oxide on silicon substrates. We have also studied silicon nitride and high-pressure-grown silicon dioxide. The techniques and apparatus that we have developed under this program are, moreover, immediately applicable to the study of other types of insulating films and substrates.

Chapter 2 of this report is a preprint of a paper by Genda Hu and Walter C. Johnson entitled, "Relationship Between Trapped Holes and Interface States in MOS Capacitors." This paper presents, in a more complete and useable manner, certain material that was given in a preliminary fashion in Report NVL-0059-009.

Chapter 3 is a preprint of a paper by Ching-Shi Jenq, Genda Hu, and Walter C. Johnson entitled, "Determination of Interface-State Densities in MIS Capacitors at Low Temperatures." This preprint presents, in more convenient and useable form, a technique that was previously described in a preliminary way in Reports NVL-0059-005 and -007.

In Chapter 4, Steven Jost describes preliminary results obtained in an experiment which he has proposed for using Auger spectroscopy to examine the $Si-SiO_2$ interface. His idea is to conduct the Auger analysis as the oxide is grown on a clean silicon substrate. He hopes by this means to obtain information about the structure and defects of the interfacial region. The effects of annealing will be examined. In his present

experiments he observes that as the oxidation proceeds, an Auger peak appears which does not correspond to either Si or SiO_2, and this is attributed to the transition region at the interface.

In Chapter 5, S.S. Li presents the results of further studies of high-field effects in the metal - aluminum oxide - silicon system. In the temperature dependence of the high-field injected current he finds evidence that the electrons injected into the oxide first tunnel into defect states near the oxide interface, following which these states are emptied principally by thermal emission at room temperature, or principally by tunneling or hopping at liquid nitrogen temperature. The application of high fields (4-6 MV/cm) with the field plate negative is found to result in localized regions of positive charge near the Si-Al_2O_3 interface. When the polarity of the field plate is reversed, the dielectric strength of the insulator is found to be much impaired, possibly because the localized positive regions then serve as regions of high electron injection. In this chapter, Mr. Li also summarizes his results on the breakdown strength of our samples of Al_2O_3, and he interprets the results for different temperatures, different field-plate metals, and for the two polarities of applied voltage.

2. RELATIONSHIP BETWEEN TRAPPED HOLES AND INTERFACE STATES IN MOS CAPACITORS

(Genda Hu and Walter C. Johnson)

ABSTRACT

MOS capacitors with dry-grown oxides, when stressed at fields of 7.1 - 7.5 MV/cm with field plate positive at 90°K, showed buildup of trapped holes. Interface states appeared only after the samples were warmed. The number of interface states generated in one hour at either 20°C or 66°C was linearly proportional to the original number of trapped holes. The number of states generated during one year's storage at room temperature was essentially equal to the original number of trapped holes, indicating a one-to-one cause-and-effect relationship.

Ionizing radiation produces two principal effects in metal-silicon dioxide-silicon (MOS) structures:[1] (a) Hole-electron pairs are produced in the oxide; the electrons are swept out, and some of the holes are trapped near the $Si-SiO_2$ interface.[2] (b) New electronic states are produced at the $Si-SiO_2$ interface. The effects are enhanced if a positive bias voltage is applied to the metal field plate during irradiation. Gamma rays, X rays, UV light, and electron irradiation have all been found to produce the same outcome.[1,3,4] High field stress greater than about 6.8 - 7.0 MV/cm produces similar results,[5,6] the source of the holes being impact ionization caused by hot electrons in the oxide.[7,8] It has been suggested[3,9] that the trapped holes may be responsible for the interface-state generation. Winokur et al[10,11] have produced evidence in favor of this point of view by showing that after a brief pulsed electron-beam irradiation of an MOS capacitor at room temperature, most of the holes had been transported to the interface in one second, whereas the generation of interface states continued for times as long as 10^6 sec. In this paper we give quantitative evidence of a cause-and-effect relationship between the trapped holes and the interface states generated in our high-field-stressed dry-oxide samples. We show that the number of interface states generated in a fixed time bears a linear relationship to the number of trapped holes and that the number of states eventually generated is essentially equal to the original number of trapped holes.

When the charging effects of interface states and trapped holes occur together, it is not possible to separate them, for a set of donor-like states can produce the same result as a set of acceptor-like states accompanied by a fixed positive charge. This difficulty can be overcome

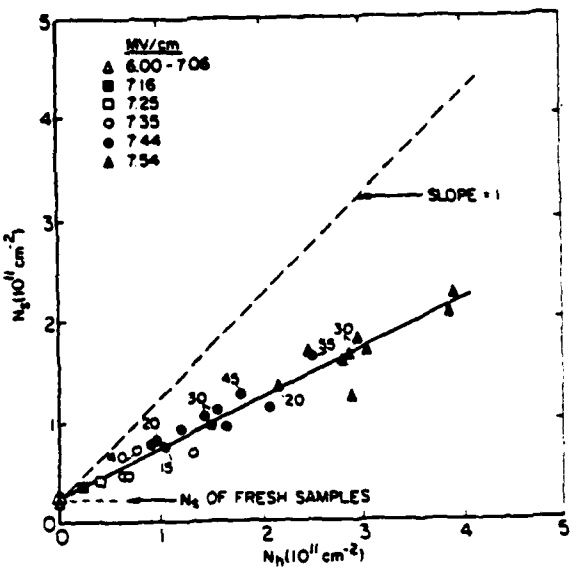
by generating the holes and measuring their concentration at low (e.g., liquid-nitrogen) temperature, for at such temperatures the generation of interface states is inhibited.[5,6,12] The sample is then warmed to allow the generation of interface states to proceed.[12]

The density of interface states was measured by a refinement of a previously described method.[6,13] Two C-V curves are taken at liquid nitrogen temperature, one with electrons frozen into the interface states and the other with holes frozen into the states. The two C-V curves have parallel portions that differ by a translation along the voltage axis owing to the different amounts of charge at the interface. The method includes all interface states except those so close to a band edge that they can emit their charge carriers during the short time required to record the C-V curve (~0.2 eV for a few seconds at 90°K).[13] The number of interface states per unit area is given by $N_s = C_i \Delta V/e$, where C_i is the insulator capacitance per unit area, ΔV is the translation between the two curves, and e is the magnitude of the electronic charge.

Our samples were MOS capacitors with n-type (100) Si substrates of 5-10 Ωcm resistivity. The oxide films were grown in dry O_2 with 3% HCl at 1000°C to a thickness of 1190 Å and were annealed in argon at 1000°C for 30 min. The field plates were of Al and were about 120 Å in thickness to permit weak-spot breakdowns to be self-quenched.[14] Bias-stress-temperature measurements showed that sodium contamination was negligible. In our experiments the samples were cooled to 90°K and were high-field stressed with the field plate positive in polarity to keep the substrate in accumulation. The number of trapped holes was varied from sample to sample by using different stress fields and

times of stressing. The stress fields were in the range 6.0 - 7.5 MV/cm and the stress times were 15-55 min. At these fields the transport of the holes to the Si-SiO_2 interface is reasonably rapid, even at 90°K.[15] C-V curves of the type described in the preceding paragraph were taken both before and after stressing to check for interface states and also to determine, by the shift in flatband voltage, the concentration of stress-produced holes trapped at the interface. The samples were then warmed (in about 20 min.), some to 20°C and others to 66°C. After allowing the interface states to develop at these temperatures for one hour, the samples were again cooled to 90°K for measurement of the interface state densities by the method used previously. (Temperatures higher than 66°C were not used because annealing of interface states was observed even at this temperature after about 4 hrs.) Finally, some of the samples were stored in the dark in a dry atmosphere for one year at room temperature, after which measurement was made of the interface-state densities.

The results of these experiments are shown in Fig.2.1, in which the number of interface states generated after warming (N_s cm^{-2}) are plotted against the number of holes originally trapped at the interface (N_h cm^{-2}). In Fig.2.1(a) are plotted the results obtained on 29 samples which had been differently stressed at 90°K and then warmed and held at 20°C for one hour. The stress times were 25 min. unless otherwise indicated beside the plotted point. The experimental data are fitted reasonably well by a straight line with a slope of 0.5. Figure 2.1(b) shows the results obtained on 6 other samples that were held at 66°C for one hour. The straight line has a slope of approximately 0.8. Finally, in Fig.



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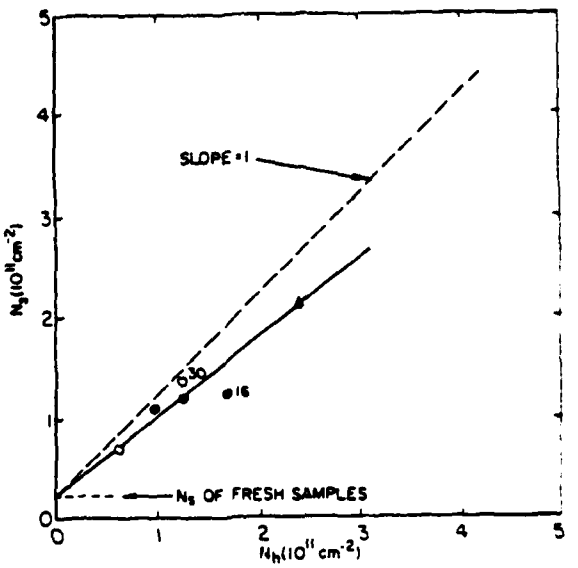

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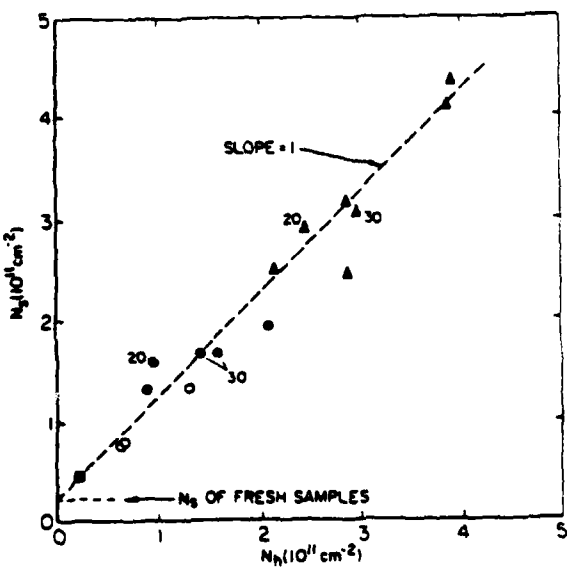

(c)

Fig. 2.1. The number of interface states ($N_s cm^{-2}$) generated after warming, plotted against the number of holes ($N_h cm^{-2}$) trapped at the Si-SiO_2 interface after high-field stress at 90°K. The time of stressing was 25 min unless otherwise noted beside the plotted point. (a) Results obtained on 29 samples after being held at 20°C for one hour. The straight line has a slope of 0.5. (b) Results obtained on 6 additional samples after being held at 66°C for one hour. The slope of the straight line is 0.8. (c) Results obtained after storage at room temperature for one year.

2.1(c) are shown the results obtained after storage at room temperature for one year. The data are reasonably well fitted by the straight line with a slope of unity. Preliminary results obtained on X-irradiated samples show results similar to the foregoing.

The linear relationship between trapped holes and the number of interface states subsequently generated is strongly supportive of the point of view that a cause-and-effect relationship exists between the two. The apparent straight-line relationship with a slope of unity obtained after a year's storage suggests that each trapped hole eventually produced an interface state. The interesting question of whether a hole is annihilated when an interface state is formed cannot be answered definitely from these data. The flatband voltage does indeed relax toward its initial value, but the previously mentioned difficulty in separating the charge effects of holes and interface states when the two are present simultaneously makes it difficult to draw a conclusion in this regard.

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3. DETERMINATION OF INTERFACE-STATE DENSITIES IN MOS CAPACITORS AT LOW TEMPERATURES

(Ching-Shi Jenq, Genda Hu, and Walter C. Johnson)

3.1 Introduction

During the course of an investigation of the effect of low temperatures on the high-field generation of interface states in metal-silicon dioxide-silicon capacitors [1], we found it necessary to have a method for measuring interface-state densities at low (e.g., liquid nitrogen) temperatures. The usual methods of measuring interface-state densities rely on a condition of equilibrium between charges trapped in the interface states and a Fermi level which is determined by the semiconductor bulk. A portion of the band gap is explored by varying the position of the Fermi level at the interface, either by changing the voltage applied to the MOS structure [2]-[6] or by varying the temperature [7]. We could not use either of these methods, firstly because thermal equilibrium is virtually impossible to achieve in silicon at liquid nitrogen temperature except for those states quite near the majority-carrier band edge, and secondly because we wished to make the measurements without increasing the temperature of the samples. As will be described here, however, it is feasible to make use of the lack of thermal equilibrium and utilize the freeze-in of carriers in the interface states to obtain a measurement of the density of such states. Brown and Gray [8] and Geotzberger and Irwin [9] have already reported on the observed shape of the low-temperature C-V curves. They have identified the various portions of the curves and have analyzed certain of the segments.

3.2 Principle of the Method

In this method, two C-V curves are taken at liquid nitrogen temperature, one with electrons frozen into the interface states and the other with holes frozen into the states. The two C-V curves have parallel portions that differ by a translation along the voltage axis owing to the different amounts of charge at the interface. The measurement includes all interface states except those so close to a band edge that they can emit their charge carriers during the short time required to record a C-V curve (~0.2eV for a few seconds at 90°K). The number of interface states per unit area is given by

$$N_s = \frac{C_{ox}\Delta V}{q} \tag{3.1}$$

where C_{ox} is the oxide capacitance per unit area, ΔV is the translation in volts between the two curves, and q is the magnitude of the electronic charge. It will be recognized that the result given by (3.1) is equal to the integral with respect to energy of the usual density of interface states, N_{ss} cm^{-2} eV^{-1}, over the energy range in which the charges are frozen into the states.

Figure 3.1 shows typical high-frequency (1 MHz) C-V curves taken at liquid nitrogen temperature on an MOS capacitor with an n-Si substrate. The capacitor is first biased into accumulation at Point A to fill the interface states with electrons. The bias is then swept from A into deep depletion at D, typically at a speed which will enable the sweep to be completed in a few seconds. Except for interface states near the conduction band edge, which can be emptied of electrons very rapidly, the electrons will be frozen into the states during this sweep. The sweep is stopped at Point D and the capacitor is temporarily illuminated with visible light to flood the interface with holes. This takes the capacitor out of deep depletion and increases the capacitance (Point E). The interface states now capture holes and go into their more positive charge condition. When the illumination is removed, the capacitance drops (Point F) as excess holes at the interface drift into the substrate. The bias voltage is now swept from Point F toward Point A. This applies a forward bias to the space-charge region of the semiconductor and causes a current of holes to flow in much the same fashion as in a p-n junction [9]. As we show later, this current of holes is such a sensitive function of surface potential that the potential changes very little as the holes are forced out, and therefore the capacitance from Point F to Point G changes very little.

By the time Point G has been reached, the interface has been depleted of holes. However, except for states so near the valence band that they can emit their holes quickly, holes will be frozen into the interface states and the states will therefore remain in their more positive charge condition. This causes the segment GH to be located to the left of the segment BC in which these same states were in their more negative charge condition. This observation provides us with (3.1).

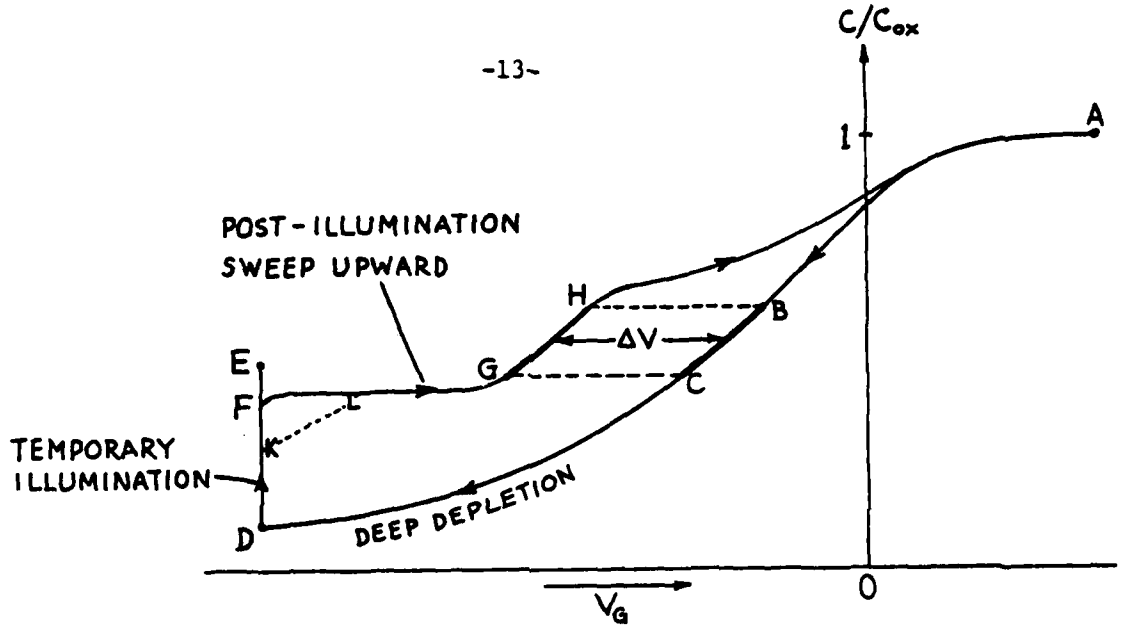

FIG. 3.1. Typical deep-depletion and post-illumination C-V curves taken at liquid-nitrogen temperature.

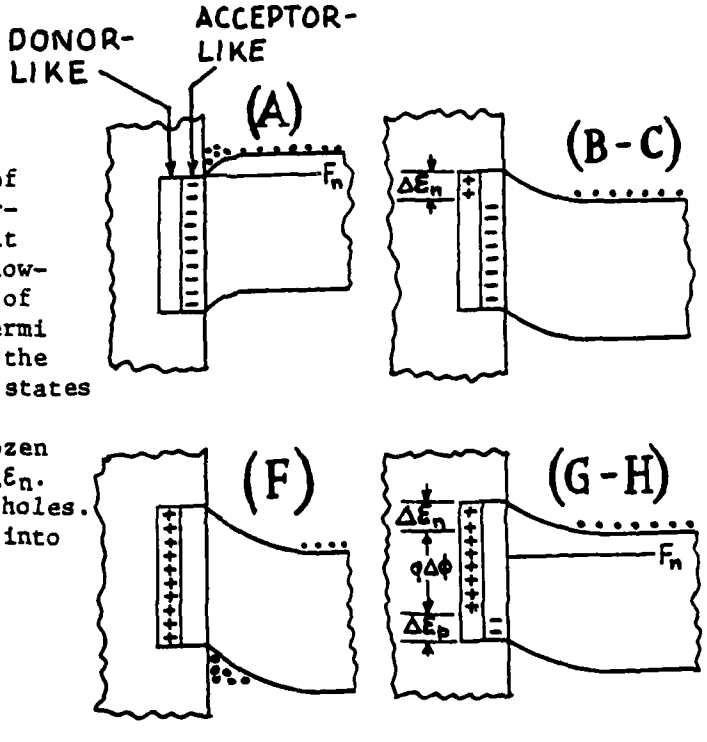

FIG. 3.2

The charge conditions of donor-like and acceptor-like interface states at various points on the low-temperature C-V curves of Fig. 3.1. F_n is the Fermi level for electrons in the semiconductor. (A) All states capture electrons. (B-C) Electrons are frozen into the states below $\Delta\mathcal{E}_n$. (F) All states capture holes. (G-H) Holes are frozen into the states above $\Delta\mathcal{E}_p$.

At Point H the electron density at the interface has increased to the point where electron capture by the interface states has become important, and above Point H the states that had holes frozen into them revert to their more negative charge condition by capture of electrons.

A further detail is shown in Fig. 3.1. If the amount of illumination is reduced, fewer holes will be produced and the capacitance may rise only a point such as K. When the sweep to the right is started, the number of holes at the interface will remain almost constant in the beginning, resulting in a section KL which is parallel to the corresponding portion of the down-swept curve. This detail is not important in the application of the technique. The important matter is to be able to recognize the section GH that is parallel to BC.

The charge conditions of the interface states are detailed in Fig. 3.2. The letters in parentheses refer to the corresponding points on the C-V curves of Fig. 3.1. At Point A the interface is in accumulation and all of the states have captured electrons. Acceptor-like states are charged negatively, and donor-like states are neutral. As the bias is swept downward (B-C), the states near the conduction band have time to emit their electrons into this band, causing donor-like states to go positive and acceptor-like states to go neutral. As will be shown in Sec. 3.3, the energy range over which this occurs, $\Delta\varepsilon_n$, is a logarithmic function of the time allowed for emission, and therefore it is quite well defined at any particular temperature (Table 3.1). In the sweep from B to C and beyond, the charges are frozen into the states below $\Delta\varepsilon_n$ and these states are thus in nonequilibrium. After completion of the sweep into deep depletion, the capacitor is illuminated and the interface is flooded with holes. The interface states capture holes and, at point F, the donor-like states are positive and the acceptor-like states are neutral. The sweep from F to G forward-biases the depletion region of the semiconductor and causes the holes to be expelled into the bulk. The states near the valence band have time to emit their holes into this band, resulting in the charge condition shown at G-H. Again, the energy range $\Delta\varepsilon_p$ is well defined owing to its logarithmic dependence on the time allowed for emission. The interface charges are frozen into the condition shown at G-H until the Fermi level for electrons, F_n, rises to the point where the electron density at the interface is sufficiently

great to permit electron capture within the time allowed by the sweep. States below F_n then capture electrons and go into their more negative charge condition. The upward sweep eventually takes the interface into accumulation again at Point A. We refer again to Fig. 3.2. Comparison of the charge conditions at G-H and B-C shows that all interface states have changed their charge condition within the central region of the band gap above $\Delta\epsilon_p$ and below $\Delta\epsilon_n$. Furthermore, all of these states, whether donor-like or acceptor-like, are more positive in G-H than in B-C. The translation ΔV in Fig. 3.1 therefore includes the effect of both donor and acceptor states, and N_s in Eq. (3.1) includes the sum of both types. The energy range over which the freeze-in is effective is

$$q\,\Delta\phi = \epsilon_g - (\Delta\epsilon_n + \Delta\epsilon_p) \tag{3.2}$$

where $\Delta\phi$ is in eV and ϵ_g is the width of the gap. The average density of interface states in the energy range $\Delta\phi$ is given by

$$\bar{N}_{ss} = \frac{C_{ox}\Delta V}{q\,\Delta\phi} \quad \text{per unit area per eV.} \tag{3.3}$$

3.3 Other Relationships

Aside from the basic equations (3.1)-(3.3), there are several quantitative relationships that are of importance. The first of these deals with the energy range over which charge carriers are frozen into the interface states at a particular temperature. The mean time for emission of an electron from an interface state is given by [10]

$$\tau_{En} = \frac{1}{v_n \sigma_n N_c} \exp[(\epsilon_c - \epsilon_s)/kT] \tag{3.4}$$

where v_n is the thermal velocity of free electrons, σ_n is the capture cross section for electrons, N_c is the effective density of states in the conduction band of the semiconductor, $\epsilon_c - \epsilon_s$ is the depth of the interface state below the edge of the conduction band, k is Boltzmann's constant, and T is the absolute temperature. In Eq. (3.4) we place $\epsilon_c - \epsilon_s = \Delta\epsilon_n$ and τ_{En} equal to the time allowed for emission of electrons, Δt_{En}; i.e., the time required to sweep the bias voltage from accumulation

to Point B. We then obtain the following expression for $\Delta\varepsilon_n$:

$$\Delta\varepsilon_n = kT \ln (v_n \sigma_n N_c \Delta t_{En}) \tag{3.5}$$

Because the argument of the logarithm is much greater than unity, the value of $\Delta\varepsilon_n$ is insensitive to changes in the argument. This is shown in Table 3.1, where we have assumed T = 80°K, $v_n = 5\times10^6$ cm/sec, and $N_c = 4\times10^{18}$ cm^{-3}. It will be seen that $\Delta\varepsilon_n$ is quite well defined even when Δt_{En} is ill defined and σ_n is not accurately known. The method relies for its usefulness on this fact.

TABLE 3.1. Values of the energy range for electron emission at 80°K

$\sigma_n(cm^2)$	Δt_n(sec)	$\Delta\mathcal{E}_n/q$(eV)
10^{-15}	1	0.16
	2	0.17
	4	0.17
	8	0.18
10^{-13}	1	0.19
	2	0.20
	4	0.20
	8	0.21

A relation similar to Eq. (3.5) gives the energy range for hole emission shown as $\Delta\mathcal{E}_p$ in Fig. 3.1:

$$\Delta\mathcal{E}_p = kT \ln(v_p \sigma_p N_v \Delta t_{Ep}) \tag{3.6}$$

where v_p is the thermal velocity of free holes, σ_p is the capture cross section for holes, N_v is the effective density of states in the valence band of the semiconductor, and Δt_{Ep} is the time allowed for the emission of holes. Owing to the insensitivity of the logarithm to its argument, the values given in Table 3.1 can be used for $\Delta\varepsilon_p$ also. If, as has often been conjectured, the states in the upper half of the gap are acceptor-type and those in the lower half of the gap are donor-type, σ_n

of the former and σ_p of the latter would both be expected to be of the order of 10^{-15} cm^2. As is shown in Table 3.1, the values of both $\Delta\varepsilon_n/q$ and $\Delta\varepsilon_p/q$ would then be expected to be very close to 0.17 eV at 80°K. The energy gap of silicon is approximately 1.18 eV at this temperature, and so from (3.2) we calculate, approximately, $\Delta\emptyset = 1.18 - 2 \times 0.17 = 0.84$ eV at 80°K. As is shown by (3.5) and (3.6), the effect of higher temperatures is to increase both $\Delta\varepsilon_n$ and $\Delta\varepsilon_p$ and thus reduce $\Delta\emptyset$, all approximately in a linear manner. This temperature dependence provides the possibility of using this method to determine N_{ss} as a function of energy in the gap. However, it should be recognized that as $\Delta\phi$ is made smaller, the uncertainty in the value of $\Delta\phi$ becomes larger.

It is shown in the Appendix that the surface potential required to expel the holes from the interface (Segment FG in Fig. 3.1) is given approximately by

$$\psi_{Ep} = 2\frac{kT}{q}\ln\left(\frac{\pi}{4\sqrt{2}}\frac{\Delta t_{Ep}}{\tau_o}\sqrt{\frac{kT/q}{\psi_{Ep}}}\right) \tag{3.7}$$

where Δt_{Ep} is the time required to expel the holes (width of the segment FG in Fig. 3.1) and τ_o is the lifetime of holes as minority carriers in the silicon substrate. Although ψ_{Ep} appears in the argument of this expression, this fact should cause no computational difficulties since the argument is much greater than unity and consequently the logarithm is not sensitive to the value of its argument. Successive approximations should yield the value quickly. Because of the nature of the assumptions used in deriving (3.7), the result can be considered to be only approximate. The effects of the parameters, however, can be seen in this equation.

At Point H in Fig. 3.1 the density of free electrons at the surface has increased to the point where electron capture by the interface states has become important, and the states begin to revert to their more negative condition. The mean time for capture of electrons is [10]:

$$\tau_{Cn} = \frac{1}{\sigma_n v_n n_s} \tag{3.8}$$

where n_s is the density of free electrons at the surface:

$$n_s = N_D e^{-q\psi_s/kT} \tag{3.9}$$

where N_D is the density of donor atoms and ψ_s is the surface potential.

Upon substituting (3.9) into (3.8), setting ψ_s equal to ψ_{Cn}, the surface potential at which electron capture becomes important, and finally replacing τ_{Cn} by Δt_{Cn}, the amount of time allowed for electron capture, we obtain:

$$\psi_{Cn} = \frac{kT}{q} \ln (\sigma_n v_n N_D \Delta t_{Cn}) \quad . \tag{3.10}$$

The value of ψ_{Cn} must be smaller than ψ_{Ep} for a parallel portion of the curve to exist. We have, however, found this condition to hold in all of our experiments at liquid nitrogen temperature.

3.4 Example and Practical Note

Figure 3.3 shows deep depletion and post-illumination C-V curves taken at 83°K on a 1030-Å oxide that had been wet-grown on an n-type Si substrate having $N_D \approx 7 \times 10^{14}$ cm^{-3}. The sweep rate was 0.4 V/sec in both directions. The voltage translation between the parallel sections of the two curves is $\Delta V = 1.18$ volts. From (3.1), $N_s = 2.4 \times 10^{11}$ cm^{-2}. Using $\Delta\phi = 0.84$ eV, Eq. (3.5) yields the average value $\bar{N}_{ss} = 2.9 \times 10^{11}$ cm^{-2} eV^{-1} in the central region of the band gap located 0.17 eV from each band edge. We conducted an analysis of the distribution of interface states using the quasi-static C-V characteristics taken by the ramp method of Castagué [11] and Kuhn [5]. The data were taken at 66°C to keep the interface in thermal equilibrium at the sweep rate of 0.4 V/sec. Utilizing Kuhn's method [5] of analyzing the data, we found that the interface-state density had a minimum of approximately 1.7×10^{11} cm^{-2} eV^{-1} near the middle of the gap and increased to about 6×10^{11} cm^{-2} eV^{-1} at energies 0.2 eV distant from both valence and conduction band edges. Owing to the inherent difficulties of using the method too close to the band edges, reliable results could not be obtained closer to the bands than this. The average density of interface states in the range E_v + 0.2 eV to E_c - 0.2 eV was computed to be 2.8×10^{11} cm^{-2} eV^{-1}, which is quite close to the value obtained by the method we are using here.

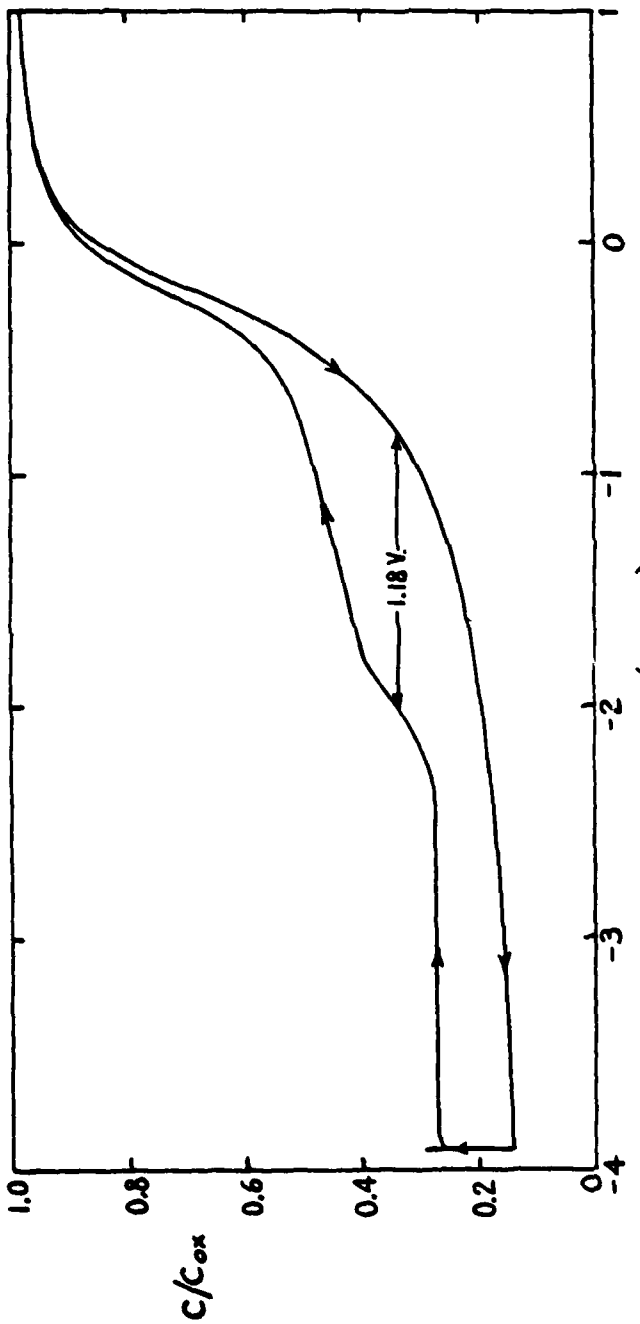

FIG. 3.3. Deep-depletion and post-illumination curves taken at 83°K on an MOS capacitor. The oxide was steam-grown to a thickness of 1030 Å on an n-Si substrate having $N_D \approx 7 \times 10^{14}$ cm^{-3}. The sweep rate was 0.4 V/sec in both directions. The voltage translation of 1.18 V indicates an average interface-state density $\bar{N}_{ss} \approx 2.9 \ 10^{11}$ $cm^{-2}eV^{-1}$ in the approximate energy range $\mathcal{E}_v + 0.17$ eV to $\mathcal{E}_c - 0.17$ eV.

Using the values $\mu_p = 1.6 \times 10^3$ cm^2/V-sec, $\tau_o = 1 \times 10^{-6}$ sec, and $\Delta t_{Ep} = 1.5$ sec, we compute $\psi_{Ep} = 0.17$ eV from (3.7). This provides the ratio $C_{Ep}/C_{ox} = 0.36$. This is somewhat higher than the value 0.28 shown in Fig. 3.3, but is perhaps within the range of error expected in view of the approximations that were made in deriving (3.7).

At this point we should mention a practical point: the value of capacitance observed when expelling holes from the interface (segment FG in Fig. 3.1) was found to depend on the history of biasing and of cooling the sample. We believe that this is the effect of ions (possibly OH^-) that are immobilized in the vicinity of the field plate at these temperatures [12]. Although ΔV in Fig. 3.1 remains the same, lowering the value of the capacitance is desirable because this provides a longer parallel portion of the curve. We have found that the capacitance can be lowered by first cooling to liquid nitrogen temperature, then warming to about 150°K with negative bias impressed on the field plate, and finally cooling again for the measurements. A possible reason for this is that the ions are rendered mobile at ~150°K and are drifted laterally to a position away from the field plate where their inversion of the substrate does not matter.

Calculation of ψ_{Cn} using (3.10) with $\Delta t_{Cn} = 0.5$ sec (the transition time between the two regions) yielded $\psi_{Cn} = 0.10$ eV and $C_{Cn}/C_{ox} = 0.42$, in reasonable agreement with the results shown in Fig. 3.3.

3.5. APPENDIX: Value of Surface Potential Required to Expel Excess Holes From the Interface

The current of holes flowing away from the interface in Segment FG of Fig. 3.1 is similar to low-level injection across a p-n junction and is determined by carrier recombination in the space-charge region. The problem is mathematically intractable unless approximations are made. Here we shall follow the procedure used by Sah et al [13] in their analysis of a p-n junction with recombination. Since recombination is most effectively done through centers located near the center of the gap, we shall assume a set of single-level centers located near the intrinsic level of the semiconductor. Equal minority-carrier lifetimes will be assumed for both electrons and holes. Calculation of the density of

minority carriers (assumed to be holes) will be done from a quasi-Fermi level which is established by the concentration of holes at the interface.

The density of free electrons in the space-charge region can be written as

$$n = N_D e^{-q\psi(x)/kT} \tag{3.11}$$

where N_D is the concentration of donor atoms (assumed uniform), ψ is the band bending in eV, and x is measured from the interface. The density of free holes in the space charge region is given by $n_i e^{(E_i - F_p)/kT}$, where n_i is the intrinsic concentration of free carriers, E_i is the intrinsic energy level at the point in question, and F_p is the quasi-Fermi level for holes. Denoting p(0) by p_s and $\psi(0)$ by ψ_s, this can be written as:

$$p = p_s e^{-q[\psi_s - \psi(x)]/kT} \tag{3.12}$$

At the position where the concentrations of n and p cross, we have

$$n_x = p_x = \sqrt{p_s N_D}\, e^{-q\psi_s/2kT} \tag{3.13}$$

It then follows that

$$n = n_x e^{-q\Delta\psi/kT} \tag{3.14}$$

Here $\Delta\psi = \psi - \psi_x$, where ψ_x is the value of ψ where n and p cross. Also:

$$p = n_x e^{q\Delta\psi/kT} \tag{3.15}$$

Also, to good approximations,

$$\psi_x = \frac{\psi_s}{2} \tag{3.16}$$

and

$$\Delta\psi \simeq - E_x \Delta x \tag{3.17}$$

where Δx is the distance measured from the point where p and n cross. It is easy to establish that

$$E_x = \sqrt{\frac{qN_D\psi_s}{\varepsilon_{sc}}} \tag{3.18}$$

where ε_{sc} is the dielectric permittivity of the semiconductor. Then from (3.17) we can write

$$\frac{q\Delta\psi}{kT} = -\frac{\Delta x}{\lambda} \tag{3.19}$$

where λ is a characteristic length given by

$$\lambda = \frac{kT}{q}\sqrt{\frac{\varepsilon_{sc}}{qN_D\psi_s}} \tag{3.20}$$

We can now write (3.14) and (3.15) as

$$n = n_x e^{\Delta x/\lambda} \tag{3.21}$$

and

$$p = n_x e^{-\Delta x/\lambda} \quad . \tag{3.22}$$

For $n>>n_i$ and $p>>n_i$, and for recombination centers near the middle of the gap, the recombination rate per unit volume can be written approximately as [13]:

$$U = \frac{1}{\tau_o}\frac{pn}{p+n} \tag{3.23}$$

where τ_o is the minority carrier lifetime. Upon substituting from (3.21) and (3.22) we obtain

$$U = \frac{n_x}{2\tau_o}\ \text{sech}\ \frac{\Delta x}{\lambda} \quad . \tag{3.24}$$

The recombination current density is given by

$$J = q\int U\, dx \tag{3.25}$$

where the integral is to be taken over the space charge region. The result is not much changed by extending the limits of integration from $-\infty$ to $+\infty$, which gives the result:

$$J = \frac{\pi}{2} \frac{q}{\tau_o} \frac{kT}{q} \sqrt{\frac{\epsilon_{sc} p_s}{q\psi_s}} \, e^{-q\psi_{Ep}/2kT} \tag{3.26}$$

Here we have used ψ_{Ep} to denote the surface potential at which the holes are expelled from the interface. The density of holes per unit volume at the surface, p_s, can be expressed in terms of the concentration per unit area, P, as follows [14]:

$$p_s = \frac{qP^2}{2\epsilon_{sc}(kT/q)} \tag{3.27}$$

The recombination current density (3.26) can thus be written as

$$J = \frac{\pi}{2} \frac{qP}{\tau_o} \sqrt{\frac{kT/q}{2\psi_{Ep}}} \, e^{-q\psi_{Ep}/2kT} \quad . \tag{3.28}$$

The width of the ledge FG in Fig. 3.1 can be expressed as $V_P = qP_{max}/C_{ox}$ volts. If the time taken to traverse this ledge is Δt_p, the current, $C_{ox}dV/dt$, can be written as

$$J = \frac{qP_{max}}{\Delta t_p} = \frac{2qP}{\Delta t_p} \quad , \tag{3.29}$$

where P is the average concentration of holes per unit area during traversal of the ledge. Equating (3.28) to (3.29) and taking the logarithm of both sides, we obtain the following expression for the surface potential required to expel the excess holes from the interface:

$$\psi_{Ep} = 2 \frac{kT}{q} \ln\left(\frac{\pi}{4\sqrt{2}} \frac{\Delta t_p}{\tau_o} \sqrt{\frac{kT/q}{\psi_{Ep}}}\right). \tag{3.30}$$

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4. AUGER OBSERVATIONS OF INTERFACE STATES IN THE Si-SiO_2 SYSTEM

(Steven Jost collaborating)

We have obtained preliminary results in an Auger-analysis experiment in which a thin oxide layer is used for the investigation of interface states near the Si-SiO_2 boundary. A thin oxide is necessary because of the short escape depth ($\sim$4 Å) of the silicon $L_{23}VV$ Auger electrons. The $L_{23}VV$ signal from the SiO_2, the interfacial region, and the bulk Si can be monitored simultaneously. As the chemical bonding of the silicon atoms goes from pure Si to SiO_2, the change in the valence-band energies is considerable and the $L_{23}VV$ spectrum is shifted dramatically. This effect is shown in Fig. 4.1. One would therefore expect to observe a superposition of Si and SiO_2 spectra in a sample having a thin oxide layer. A change in bonding at the interface should show itself by chemically shifting the Si $L_{23}VV$ spectrum by a measureable amount.

We have conducted a preliminary series of experiments, utilizing facilities at the Princeton Plasma Physics Laboratory. In the first set of experiments a silicon sample was first sputter-cleaned with argon ions in a UHV system. The sample was then exposed at room temperature to oxygen at one atmosphere of pressure for approximately ten minutes. After the chamber was again evacuated, Auger analysis showed the presence of a thin layer of oxide on the Si. In addition, a peak near 81 eV was seen which did not correspond to either Si or SiO_2 (see Fig. 4.2). This is attributed to a chemical state in which the silicon atom is not bonded either to four Si or to four 0 atoms in the interface region. Figure 4.3 shows results obtained from cleaned silicon, oxidized silicon, and silicon that had been exposed to room air for several weeks. In this last case the peak at 81 eV is not evident (although it might be present below the detectable level). Similar results have been reported very recently by Morgen et al. (Appl. Phys. Lett. 34, 488, 15 April 1979) using much lower oxygen exposure levels. We eventually hope to use this technique to study oxidation and annealing processes similar to those found in the semiconductor industry. This may yield information concerning the formation and suppression of interface states in MOS structures.

In a separate series of experiments, the silicon substrate was first sputter-cleaned and oxidized as before, following which the Auger

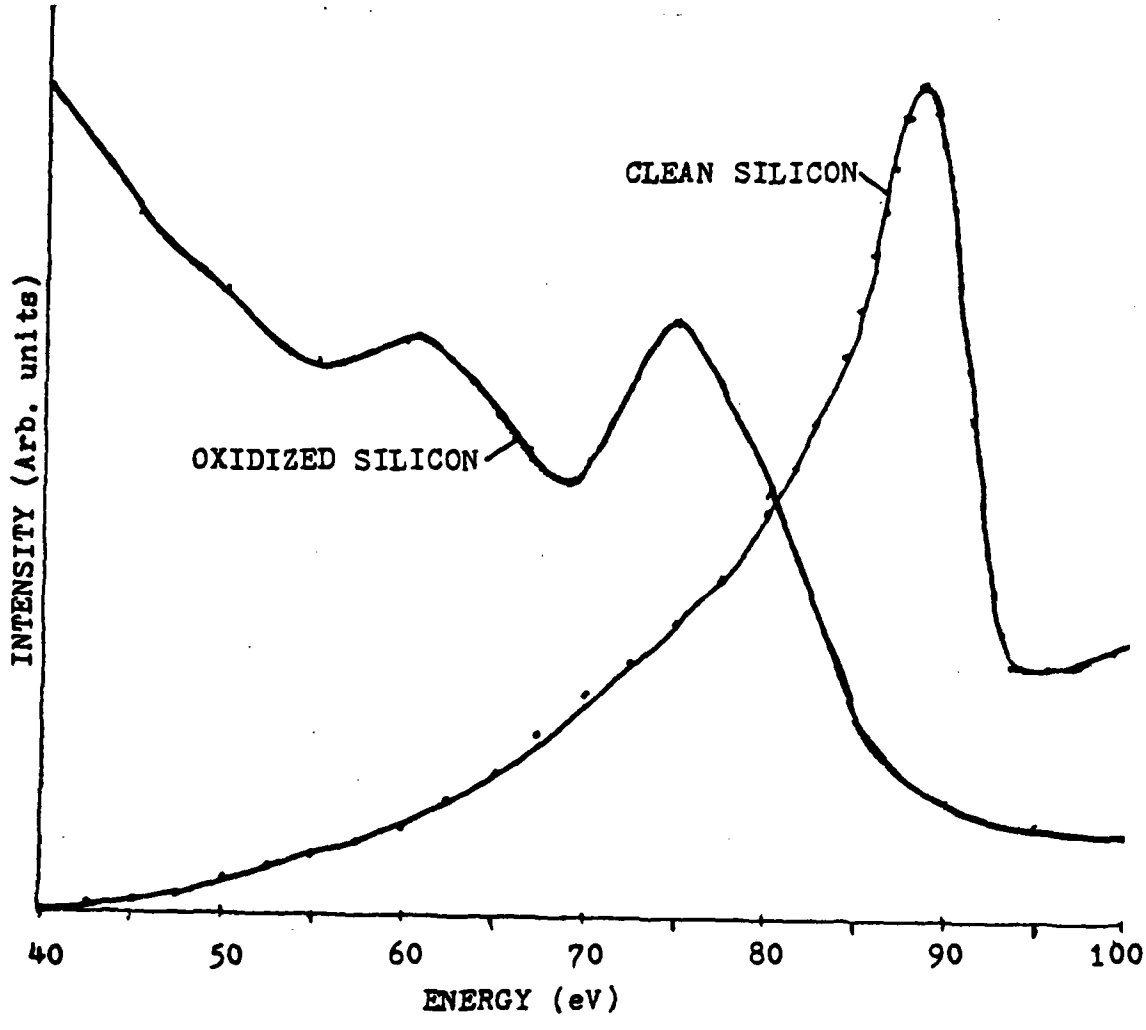

Figure 4.1. The $L_{23}VV$ spectrum of silicon for a clean substrate and for a one-micron oxide layer.

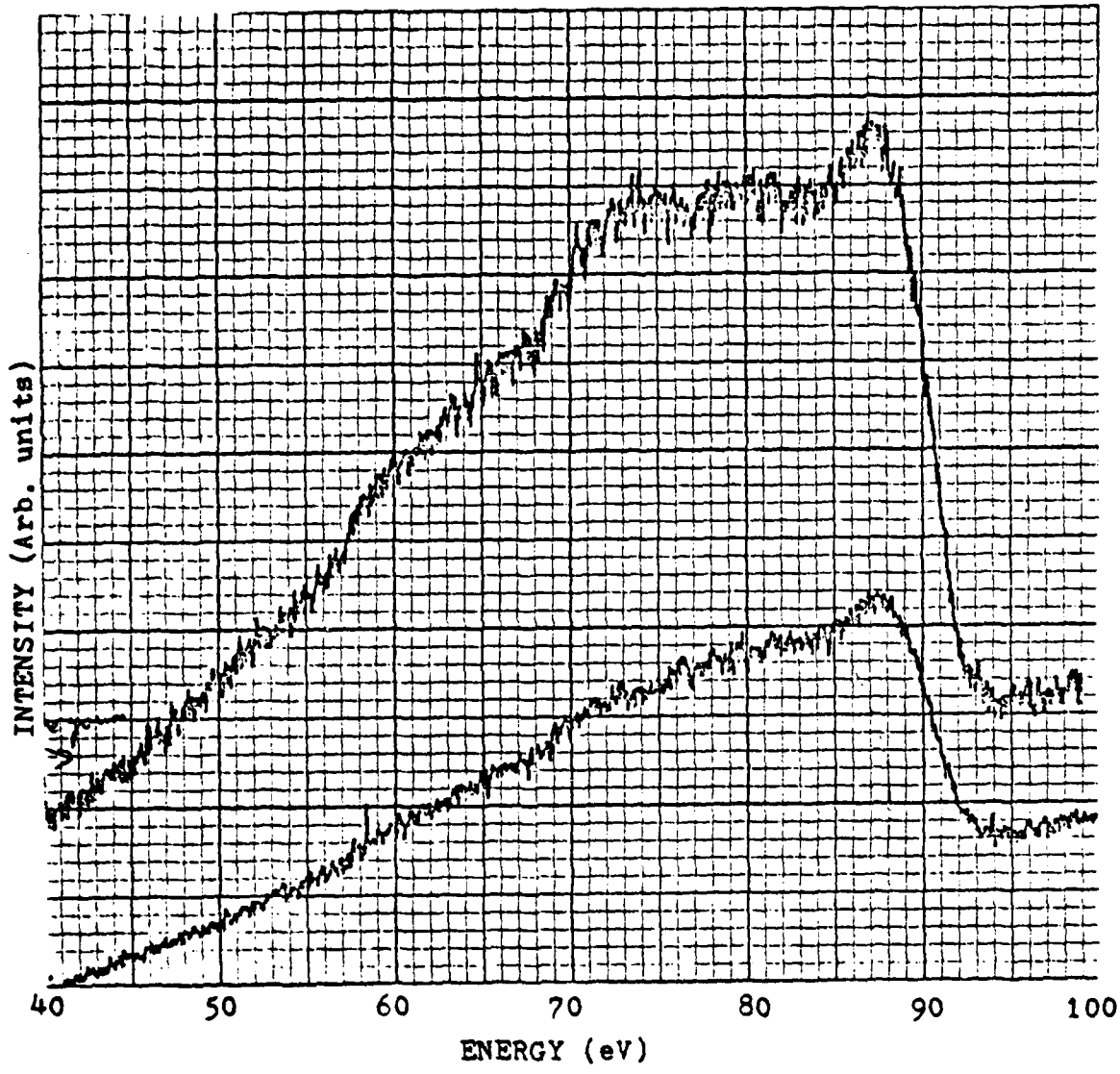

Figure 4.2. Silicon spectrum after brief oxidation at one atmosphere O_2. Upper trace is expanded version of lower trace. Note peak near 80-81 eV. This is associated with changes in the chemical bonding of the silicon near the interface.

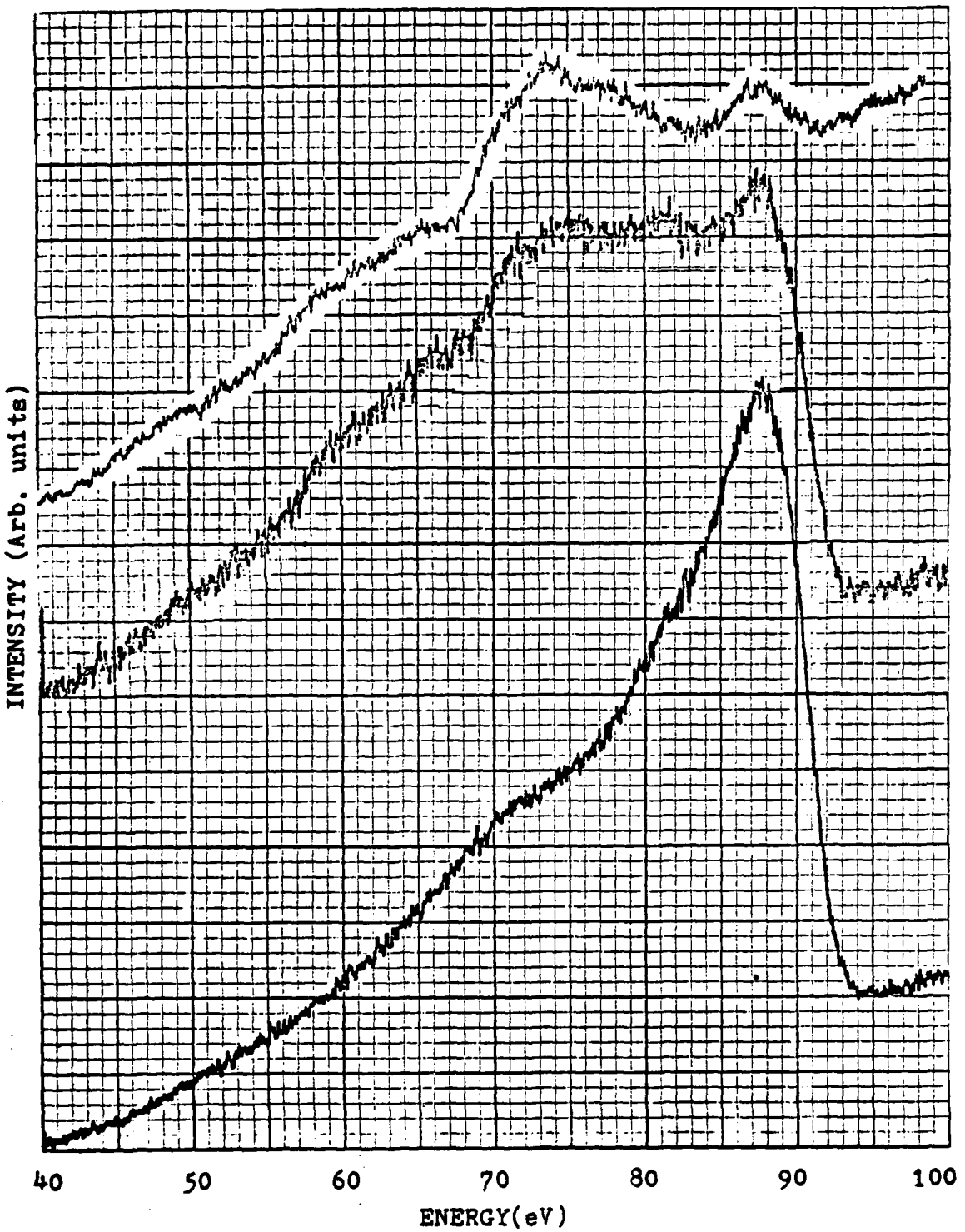

Figure 4.3. Lower trace: sputter cleaned silicon. Middle trace: oxidized silicon with new peak near 81eV. Upper trace: Sample exposed to room air for several weeks- note increase in intensity of primary oxide peak.

spectrum was examined at various times while the surface was exposed to 2×10^{-7} torr of hydrogen. This is a first approximation to the forming-gas anneal sometimes used in MOS processing. In Fig. 4.4 we see the progression from clean silicon (Curve 1) to oxidized silicon (Curve 2), followed by spectra taken after exposures to H_2. A problem with the amplifier which developed at this time prevented observation of the minor peaks as a function of hydrogen exposure. However, it is evident that the hydrogen has reduced the intensity of the pure silicon signal, indicating either a thicker oxide (which is unlikely in a UHV environment) or that the silicon spectrum is shifted to lower energies as a result of the reaction with hydrogen. Further results will be reported later.

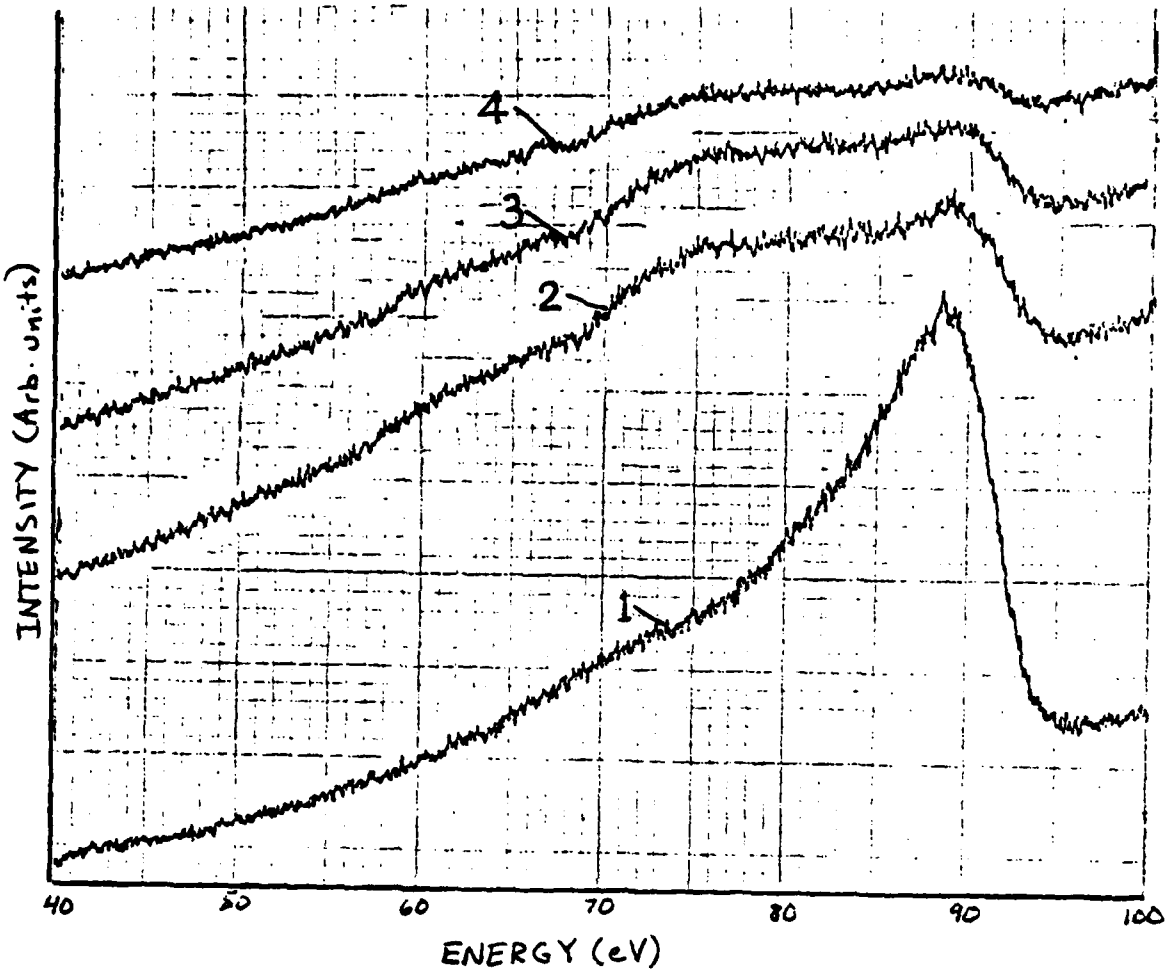

Figure 4.4. Curve 1: sputter-cleaned Si. Curve 2: partially oxidized substrate. Curve 3: oxide after exposure to 2×10^{-7} torr H_2 for 1 minute. Curve 4: oxide after exposure to 2×10^{-7} torr H_2 for 20 minutes. Note reduction in pure silicon peak and broadening of spectrum with increasing H_2 exposure.

5. FURTHER STUDIES OF HIGH FIELD EFFECTS IN METAL-ALUMINUM OXIDE-SILICON CAPACITORS

(S.S. Li collaborating)

5.1 Introduction

In this chapter we report on further studies of high field effects in the metal-aluminum oxide-silicon (MAS) system. In Sec. 5.2 we give the results of two studies. First, we show the temperature dependence of the high-field current injected from the substrate into the oxide, and from this we deduce the mechanisms involved in the injection process. Second, we show the results of experiments on charge storage and charge retention in the oxide. In Sec. 5.3 we show that high field stress applied with negative polarity of the field plate results in both electron trapping in the oxide and the formation of localized positive charge centers near the Si-Al_2O_3 interface. Interface states are formed. In Sec. 5.4 we give the results of breakdown studies of Al_2O_3 for both polarities of applied voltage at 95°K and 300°K, and for both Al and Au field plates, and we draw certain conclusions from the results. We find that our Al_2O_3 samples prepared at 815°C are inferior in dielectric strength to those prepared at 900°C. We also observe that after large negative stress, the ability of the insulator to withstand positive field stress is impaired, and we interpret this in terms of the activity of the localized positive centers, formed by negative stress, in aiding the injection of electrons from the substrate when subsequent positive voltage is applied to the field plate.

Our MAS capacitors were fabricated at Bell Telephone Laboratories by courtesy of David Boulin. The Al_2O_3 insulator was pyrolytically grown at either 815°C or 900°C to thicknesses of 450Å to 1089Å. Both n-type and p-type (100) silicon substrates were used. The substrate resistivities were in the 4-6 Ω-cm range. Semitransparent gold and aluminum field plates ("gates") were evaporated on the surface of the oxide. The gold field plates had a sheet resistivity of 5Ω/□ . The sheet resistivity of the semitransparent aluminum plates ranged from 10Ω/□ to 22Ω/□ .

5.2 Current Injection, Charge Storage, and Charge Retention

The current injection as a function of temperature was investigated. The MAS capacitors used in this experiment had n-type

silicon substrates and Al_2O_3 thicknesses of about 450Å. The samples were cooled down to temperatures ranging between 95°K to 300°K. Positive fields of 4.7 MV/cm were then applied to the capacitors. The same measurement procedure and data extraction process as described in a previous report[1] were used. A plot of measured current as a function of average field strength is shown in Fig. 5.1 for several capacitors stressed at different temperatures. The injection current as a function of interface field at different temperature is shown in Fig. 5.2. At temperatures close to 95°K, the injection current levels off, indicating that the thermally activated component of current is only a minor contribution in this temperature range. As the temperature is increased, the thermally activated component of current begins to dominate in the injected current. When the temperature is above 200°K, the log current in linearly proportional to the inverse of the temperature. The indicated activation energy is about 0.35eV.

Our interpretation of the foregoing results is as follows. The lack of temperature dependence and the strong field dependence of the injected current at temperatures below about 120°K indicates that tunneling processes limit the injection in this temperature range. With the field plate positive, electrons tunnel from the substrate into nearby defect states in the oxide and, at this low temperature, tunnel or "hop" from state to state until they reach the conduction band of the oxide. The rate of tunneling into the states nearest the interface is limited by the number of such states that are empty at any given moment, and this in turn is determined by the rate at which these states are emptied. At low temperatures, hopping into states deeper in the oxide is the only process available for emptying the states near the interface. When the temperature is raised, thermal emission aids in emptying the states and, at temperatures sufficiently high, thermal emission becomes the limiting factor.

Up to this point, our concern has been mainly on the charge build-up rate within the oxide upon long-time stressing.[2] Since MAOS capacitors can be used as charge storage devices,[11] the writing-in of the information by the impulse signal and the ability to retain this information by the capacitors are of interest. Seven Al_2O_3 MOS capacitors were

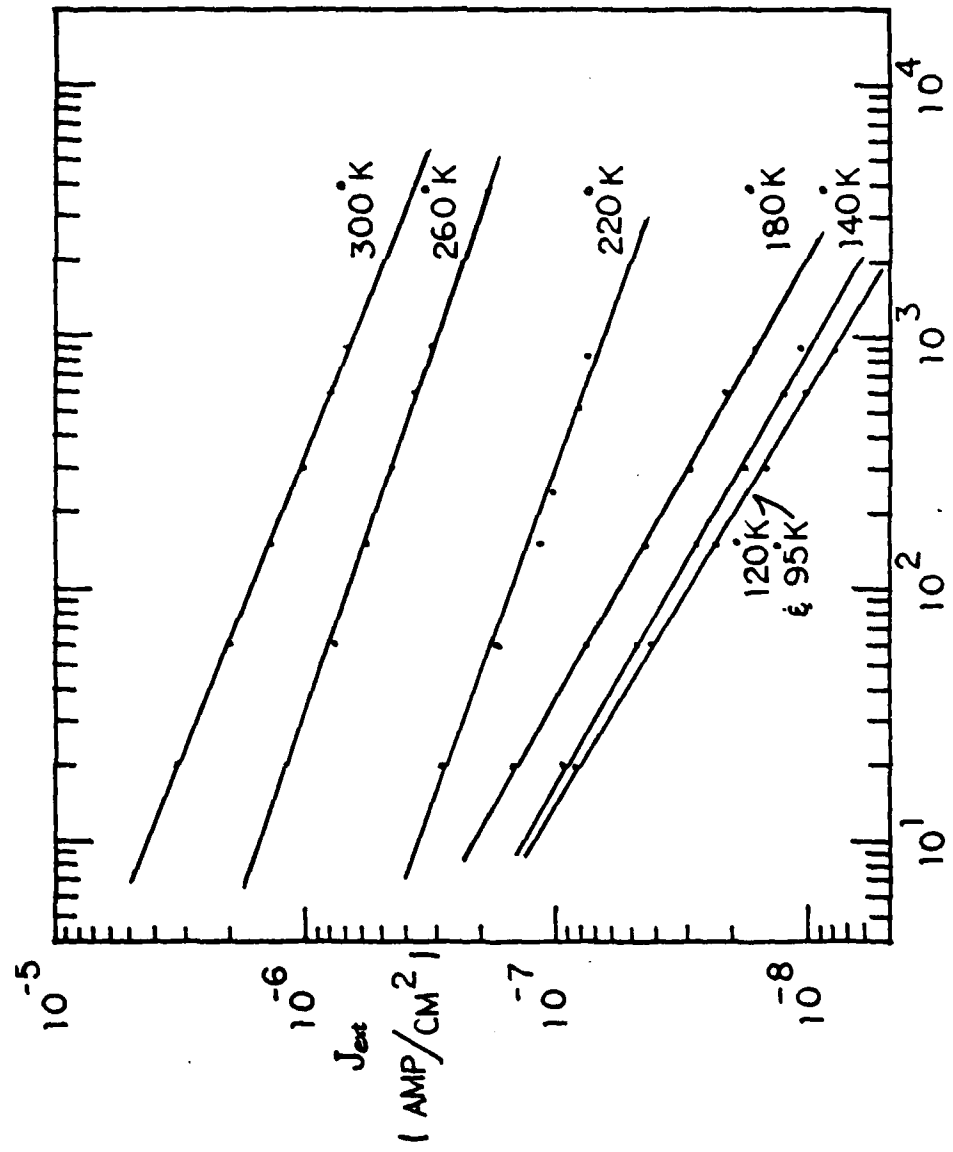

FIG. 5.1. The externally measured current as a function of time for different temperatures ranging from 95°K to 300°K. The average field applied on the capacitor was 4.7 MV/cm.

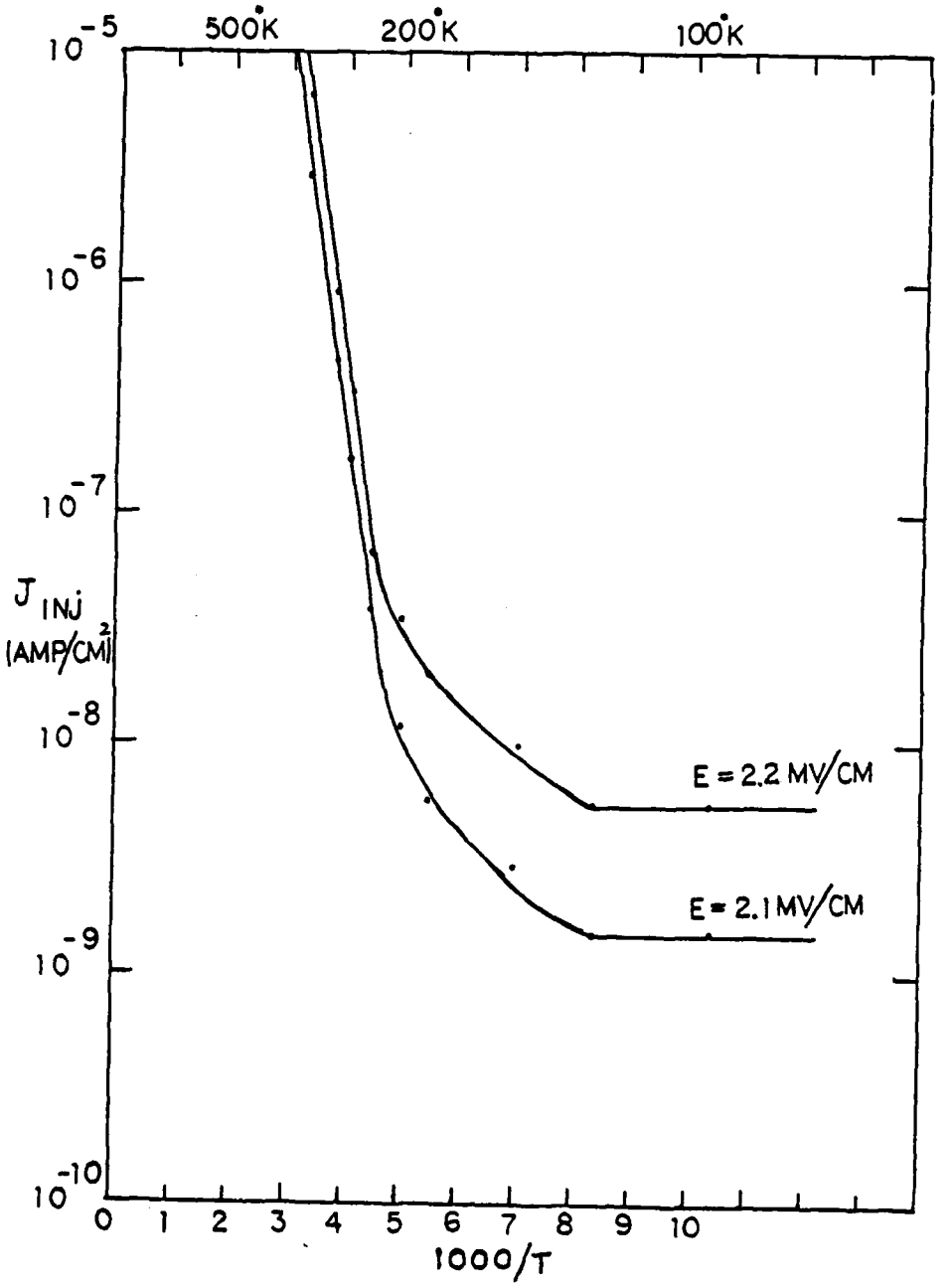

FIG. 5.2. Plot of the injected current as a function of 1/T at different interface fields.

subjected to pulsed electron injection. After each impulse, the bias on the capacitor was kept at the flatband condition so there would not be a significant loss of charge storage, and the flatband voltage was observed. The build-up of flatband voltage within the first 200 milliseconds is shown in Fig. 5.3. Here the parameter E_{IN} is the interface electric field. The duration of each impulse was equal to the time increment between successive data points in Fig. 5.3. The initial charge build-up rate is fast owing to the large capture cross section of the electron traps.[3] The charge retention ability of MAS capacitors is shown in Fig. 5.4. The charge storage in dot No. 1 was increased by impulse injection of electrons so that the flatband voltage increased to 4.52V. The capacitor was then open circuited and the flatband voltage was observed as a function of time. Curves 2-5 differ from curve 1 in that these capacitors were short circuited after charge injection. The charge storage appears to be relatively stable. The initial information loss rate is greater under short circuit conditions. The loss of a significant amount of charge captured in the interface region is observed, which was by the process of back tunneling. Additional results on the change of flatband voltage caused by the pulsed injection and trapping of electrons is shown in Fig. 5.5. Here the voltage, rather than the interface field, was held constant across the 450Å Al_2O_3. The time here is again the total time of charge injection.

5.3 Effects of Large Negative Stress

(A) Laterally Nonuniform Positive Charge and Generation of Interface States

As discussed in the previous report,[2] following negative high field stressing of the Al-field-plate MAS structure, C-V measurements first exhibit positive flatband voltage shift, showing negative charge trapping, and as the stressing time is increased, the flatband voltage shifts back, indicating a buildup of positive charge. In order to study the effect of high field stressing on the interface properties of the MAS capacitors, quasi-static C-V curves were measured on two samples designated PA-900-1 and PA-900-2. These had p-type silicon substrates with oxide thickness about 450Å. The C-V measurements were taken at

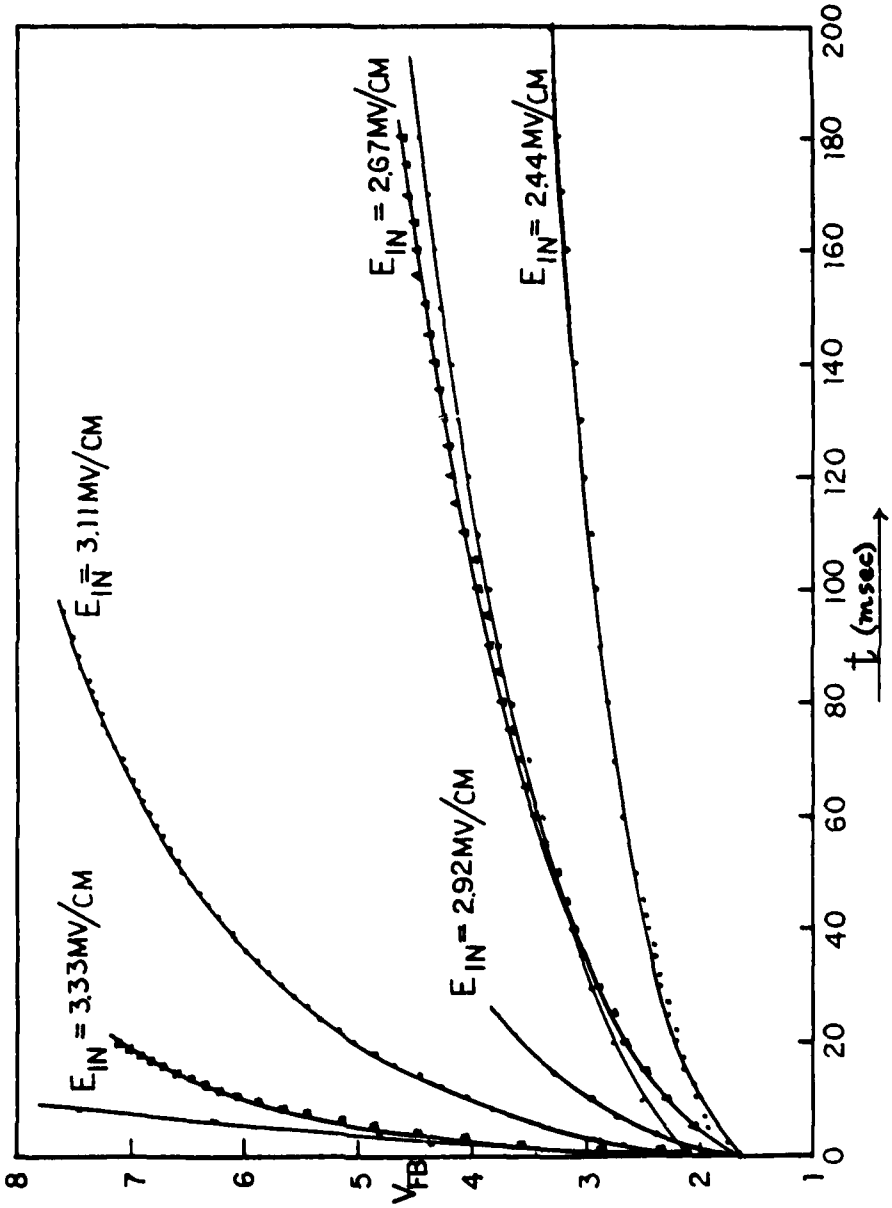

FIG. 5.3. Change of flatband voltage of MAS capacitors caused by capture of electrons following pulsed injection of electrons, plotted against the total injection time in milliseconds. E_{IN} is the interface field during injection.

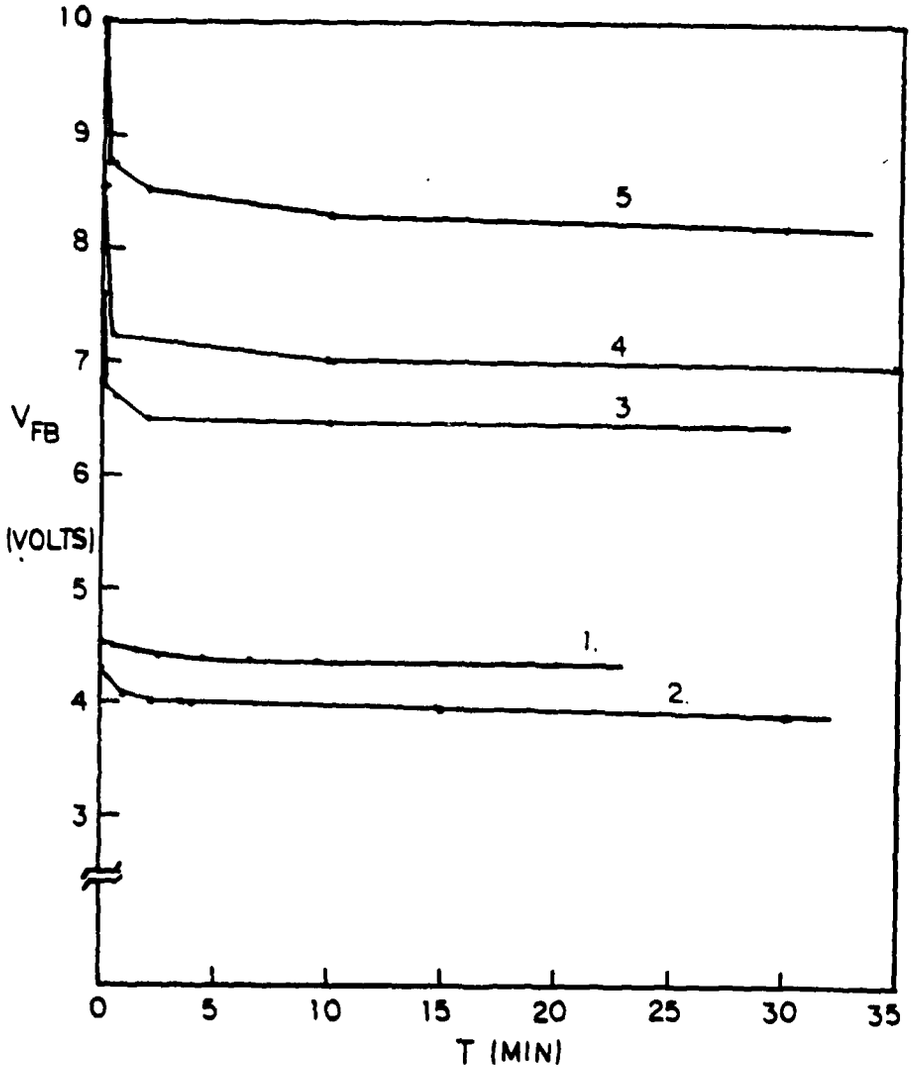

FIG. 5.4. Charge retention ability of MAS capacitors. Capacitor No. 1 was open circuited after injection and capture of electrons. Capacitors 2-5 were short circuited after electron injection.

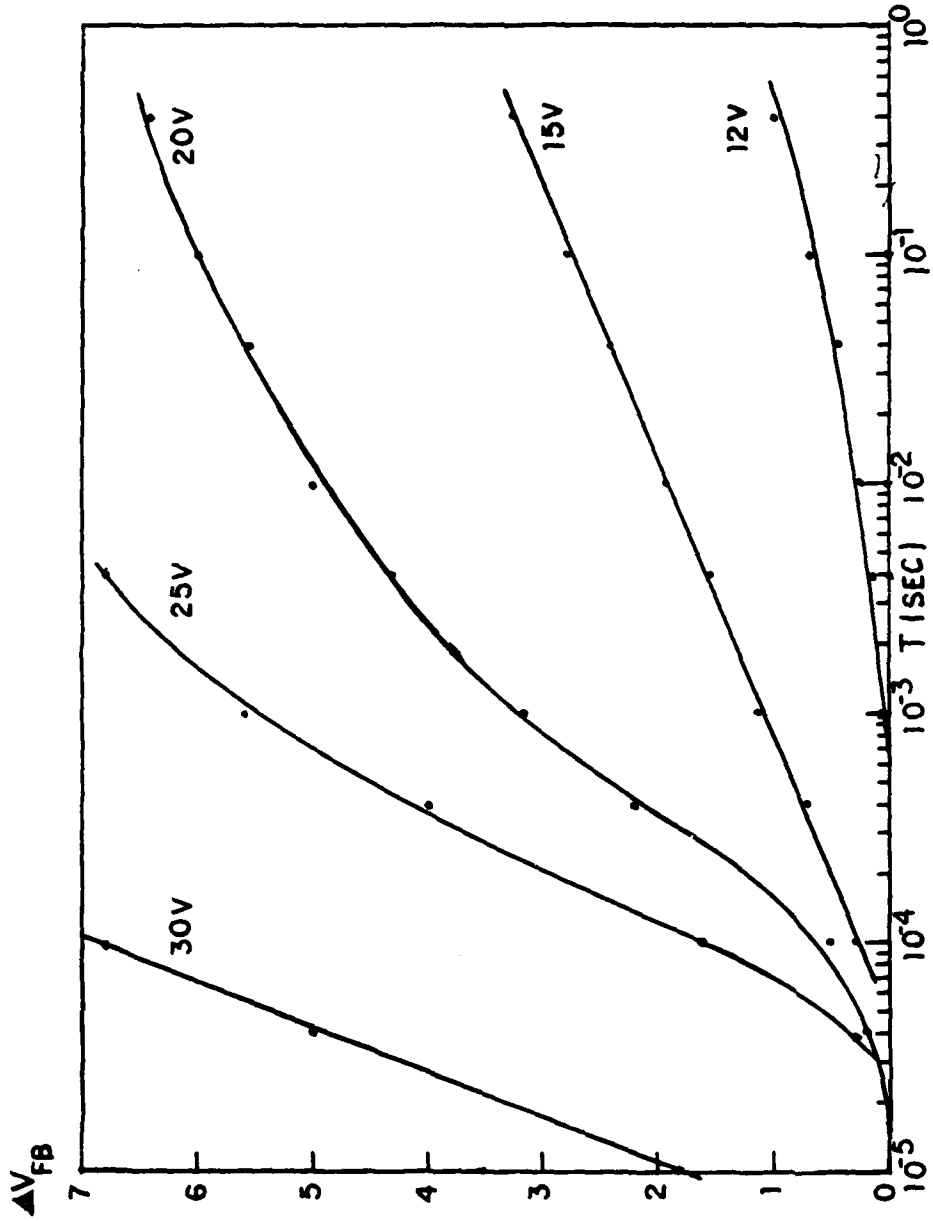

FIG. 5.5. Population of electron traps by pulsed injection of electrons into MAS capacitors.

60°C so that the minority-carrier response time would be sufficiently reduced by thermally activated processes to allow reasonable ramping rates in taking the quasi-static curve. In Fig. 5.6, Curve 1 is the quasi-static C-V curve for the fresh dot. The bump observed in this curve indicates the presence of interface states in the fresh MAS capacitors. Sample PA-900-1 was then stressed at -4,67 MV/cm for 150 minutes at room temperature. After the stressing, the C-V curve was stretched out and a significant amount of hysterisis appeared as shown in Curve 2. This hysteresis is attributed to an increase in negative trapped charge or alternatively a loss of positive charge in the oxide when the applied ramp voltage was swept from 0 volt to 5.0 volts. After the C-V curve swept back to 0 volt, a subsequent C-V curve showed the hysterisis loop and the extent of the C-V stretch-out to be decreased. This phenomenon is interpreted as follows: the negative high field stress causes a buildup of laterally nonuniform positive space charge near the interface regions. Some of positive charges located close to the interface can be recombined by the tunneling-in of electrons during the first C-V measurement; thus, the high frequency C-V curve taken the second time shows a rather smaller hysteresis loop.

If electrons are then field-injected intc the oxide, the trapping of electrons or the recombination of electrons with positive charge causes the flatband voltage to shift farther to the right side. This is shown in Fig. 5.7. For Curve 1, electrons were injected from the substrate by applying +12V to the field plate (average field 2.7MV/cm) for 5 min. The high-frequency C-V curve 1A was taken by sweeping the bias from right to left, and 1B was obtained by sweeping back. Subsequent electron injection at +14V for 5 min produced Curves 2A and 2B, and further electron injection at +16V for 5 min produced Curves 3A and 3B. Curves 1A, 2A, and 3A, obtained after electron injection, are almost parallel to each other, and the extent of C-V dispersion is reduced. A temperature test presented later indicates that after negative high field stressing, a significant portion of the stretch-out was due tc the laterally nonuniform space-charge distribution. The reduction of C-V dispersion by the subsequent positive field bias is thus expected, because the electron injection and capturing is more pronounced in a localized area where there

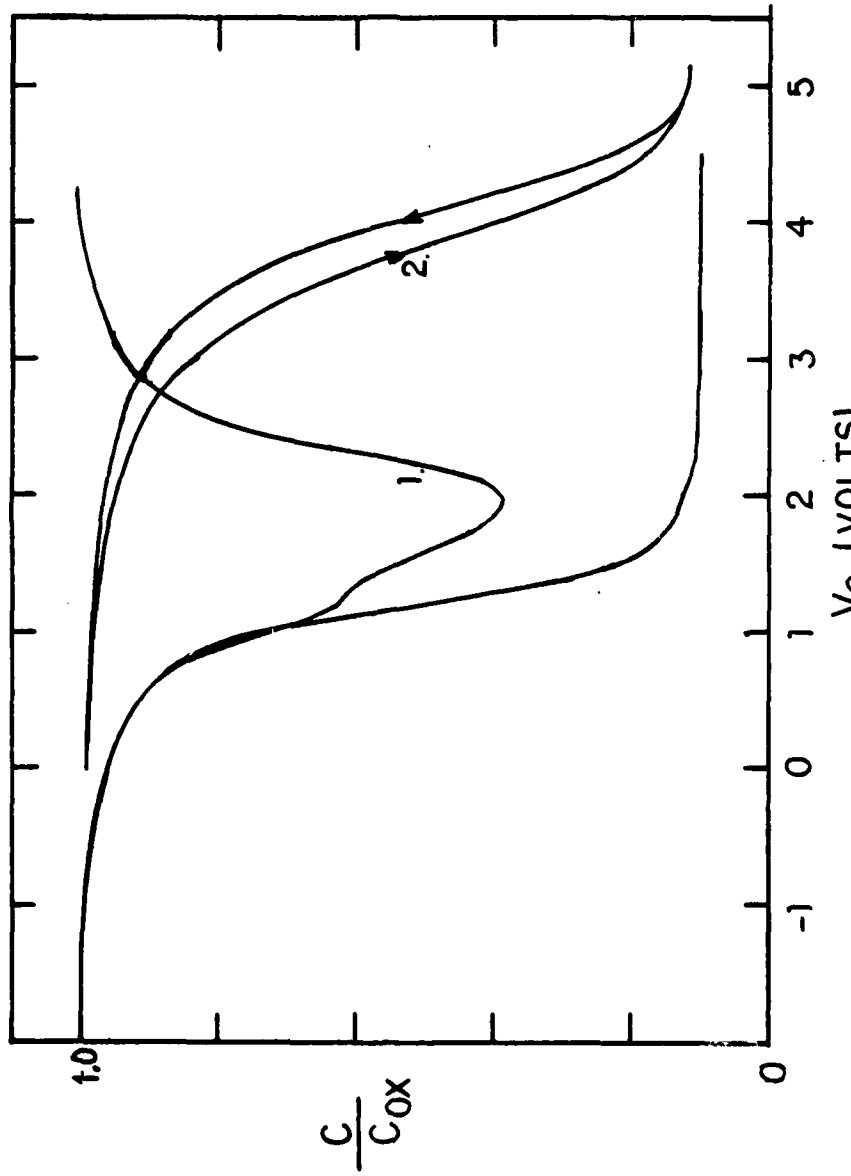

FIG. 5.6. The Effect of negative high field stress on the C-V curves of MAS capacitors.
Curve 1: High frequency and quasi-static C-V curves for the fresh sample.
Curve 2: High frequency C-V curve taken after the sample had been stressed at -4.67 MV/cm for 150 minutes.

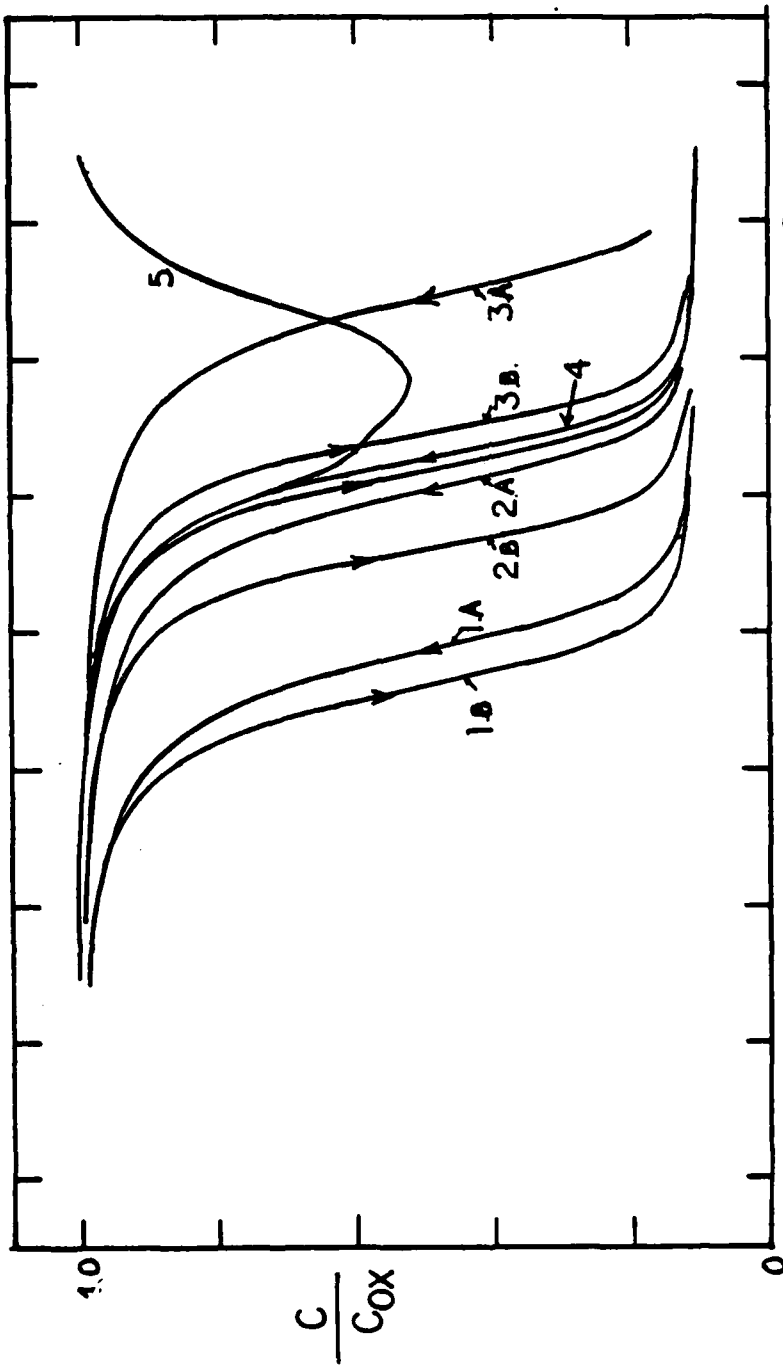

FIG. 5.7. Continuation of FIG. 5.1. After negative high-field stress of -4.67 MV for 15 min, Curves 1,2,3 were obtained by stressing the MAS capacitor at +12V, +14V and +16V for 5 minutes each. The high-frequency C-V curve was taken by sweeping from inversion toward accumulation, which induces the discharge of trapped electrons in the interface regime. Curves 1B, 2B, 3B, which were taken after this discharge, are parallel to each other. These curves are also parallel to Curve 4, which was obtained by short circuiting the MAS capacitor for an additional 20 minutes. Curve 5 is the quasi-static C-V plot taken at 60°C.

are more positive charges or less negative charges. Further electron trapping thus reduced the C-V curve distortion. Curves 1B, 2B, 3B, and 4 were obtained by discharging the captured electrons located in the vicinity of the interface. These curves are parallel to each other. The quasi-static curve was then taken and is shown as Curve 5 in Fig. 5.7. Similar results were also obtained on sample PA-900-2, which was given the larger stress of -5.11 MV/cm for 150 min. The results given in Fig. 5.8 are similar to those of Fig. 5.7.

To further test the properties of the stretched-out curves, a temperature test was utilized. Curve 1 in Fig. 5.9 was taken on a fresh MAS capacitor. After the sample was cooled down to 95°K, the deep-depletion and post-illumination curves marked 2 were taken. The post-illumination curve shows a ledge (see Ch. 3) which indicates a number of interface states in the midgap with energies of 0.21 eV away from both conduction band and valence band to be $6.1 \times 10^{11} CM^{-2}$.[4] The sample was then subjected to -5.75MV/CM for two hours. The C-V curve taken after the high field stressing was Curve 3 which is strongly distorted. At this temperature, since the interface charges were essentially frozen into the traps, the C-V curve distortion indicated that the charge storage was nonuniformly distributed in the insulator.[5] The sample was then warmed up, resulting in further stretch-out as shown by Cruve 4. To reduce the C-V stretch-out, electrons were injected into the oxide by stressing the MAS capacitor at +12 V and +14 V for 30 minutes. C-V Curves 5 and 6 were obtained after this injection. The sample was next short circuited for 160 minutes to discharge the electron traps located close to the interface region. The system was cooled down to 95°K again and the high frequency deep-depletion and post-illumination curves were taken. These are shown as Curves 7a and 7b. Curve 7a is not parallel to Curve 2, indicating that nonuniform charge storage still existed within the oxide.[5] The large hysteresis loop between 7a and 7b indicates that interface states were created after this high field stressing procedure.[4] It was also found that the large hysteresis loop appeared regardless whether the system had ever been warmed up or had instead been kept at liquid nitrogen temperature all the time. This is shown in Fig. 5.10, where the sample was subjected to negative stress and

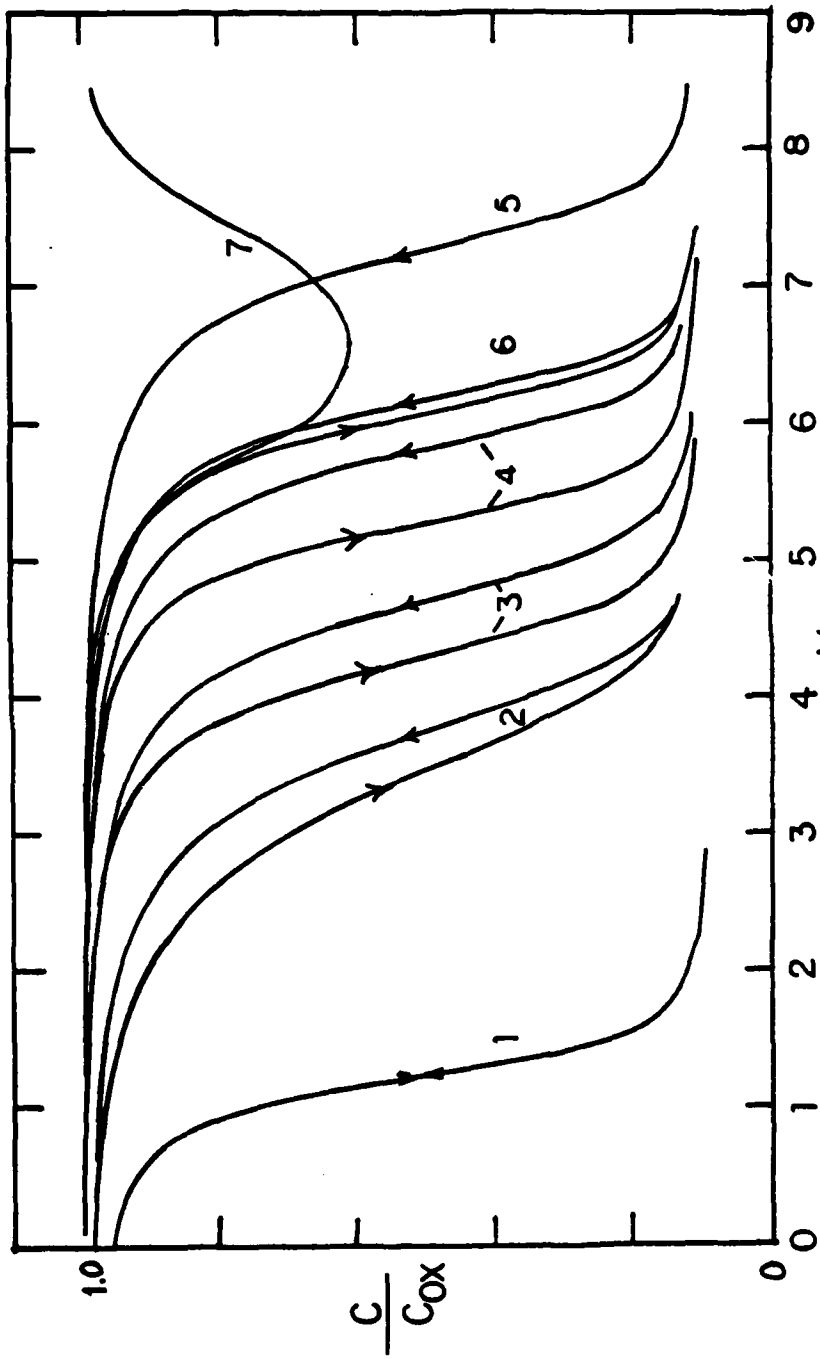

FIG. 5.8. Effect of greater negative high field stress on the C-V curves. Curve 1: High-frequency C-V curve for fresh MAS capacitor. Curve 2: Taken after the MAS sample had been stressed by -5.11 MV/cm for 150 minutes. Curves 3,4, and 5 were obtained by stressing the MAS capacitor subsequently at +12V, +14V and +16V for 5 minutes each so as to field-inject electrons from the substrate. Curve 6 was obtained by short circuiting the MAS capacitor for 20 minutes. Curve 7 is the quasi-static curve taken at 60°C.

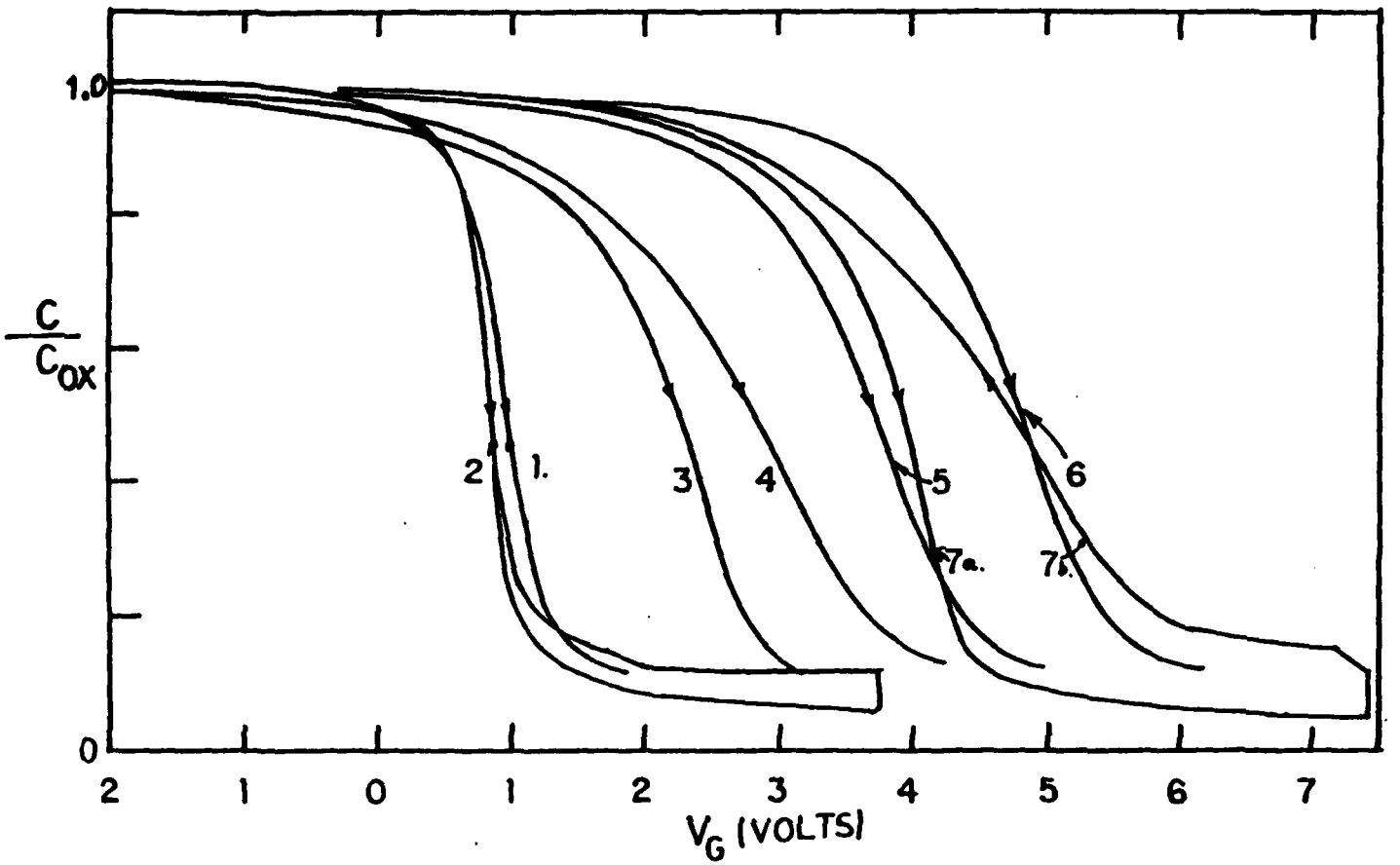

FIG. 5.9. Effect of negative high field stressing on the C-V curves. Curve 1: Taken at 25°C for fresh MAS dot. Curve 2: Taken at 95°K. Curve 3: Taken after MAS capacitor was subjected to -5.75MV/cm for 2 hours. Curve 4: Taken after MAS capacitor was warmed up to room temperature. Curves 5, 6: Obtained by stressing the capacitor at +12V and +14V for 30 minutes each to inject electrons from the substrate. Curve 7a: Taken at 95°K. Curve 7b is the post-illumination curve.

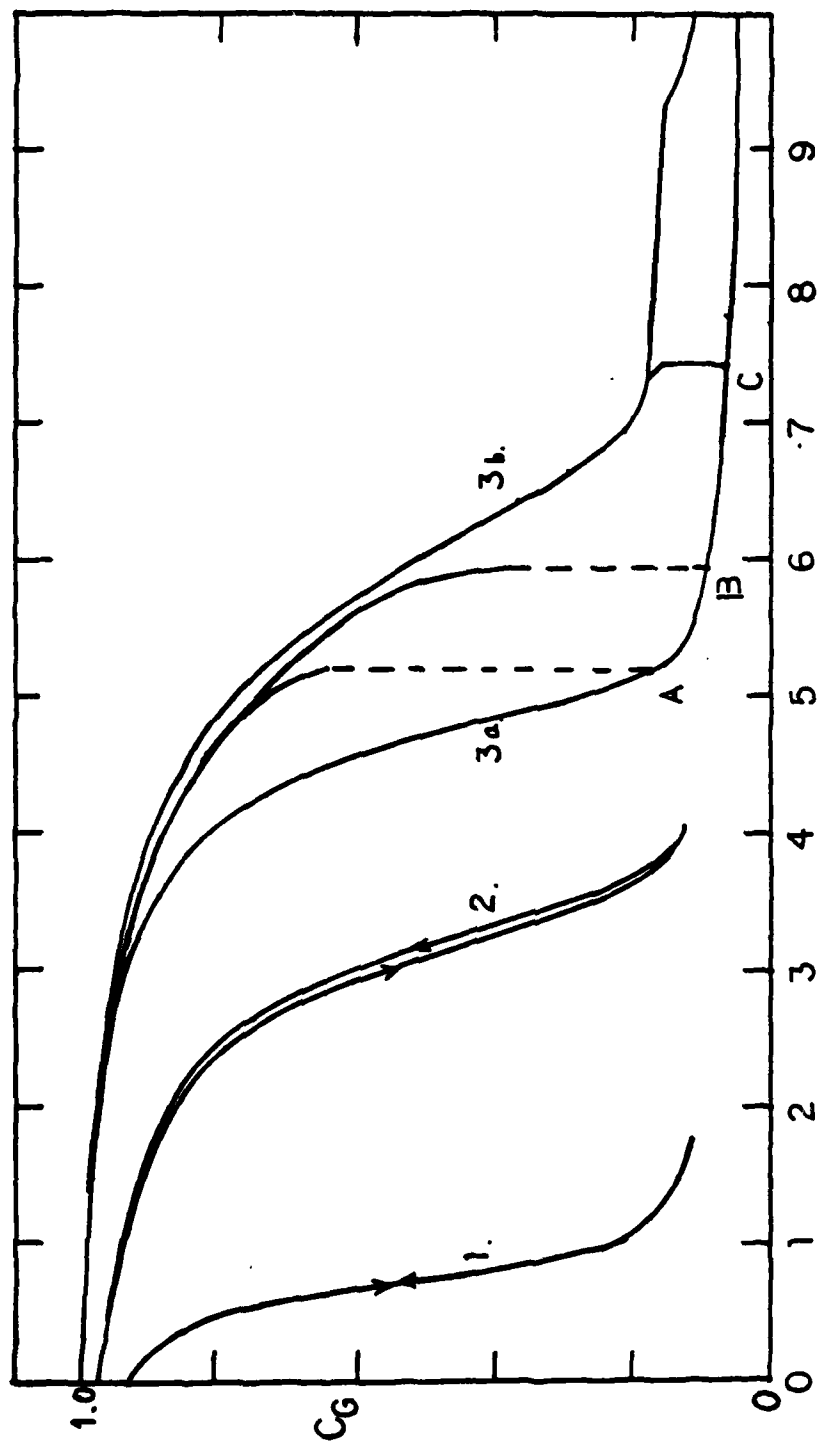

FIG. 5.10. Effect of negative high field stress on the C-V curves of an MAS capacitor kept at 95°K. Curve 1: Taken at 25°C on fresh MAS dot (for reference only). Curve 2: Taken after MAS capacitor was subjected to -5.75 MV/cm for 60 minutes at 95°K. Curve 3a: Deep depletion curve obtained after stressing the capacitor at +18V for 30 minutes at 95°K. Curve 3b: The light assisted curve measured at 95°K.

electrons were injected without warming. Curves 3a, 3b showed large hysteresis no matter whether the sample was exposed to the light at point A, point B, or point C. This indicates that for our Al_2O_3 MAS capacitors under negative high field stressing, the creation of interface states did not depend on thermal activation. In this respect they may be different from the interface states generated in the $Si-SiO_2$ system (see Ch. 2).

Owing to the presence of laterally nonuniform space charge after high-field stressing, it is very difficult to tell how many interface states are created after negative high field stressing. The large hysteresis loop which appeared in low-temperature C-V curves after high-field stressing indicates that significant amounts of interface states were generated. During the negative high-field stressing, however, a high concentration of positive charge accumulated in the oxide. A clustering of positive charges indicates that there are localized regions where electrons are missing in the valence-electron bonding structure; thus the bonding strength between atoms is locally reduced. In these regions, ions are more easily displaced. This process can be aided by the external high field stress. The local broken bonds may thus account for the localized charge-trapping sites. If these traps are accessible to the charge carriers in the silicon bands, they are regarded as newly generated interface states.

(B) Characteristics of the Positive Charges as Studied by Optical Techniques

Gold-field-plate MAS capacitors were subjected to negative high-field stressing, which, as was described in Sec. 5.3(A), eventually results in positive charging and a negative flatband voltage shift. The photodepopulation procedures for the MAS capacitors are shown in Table 5.1. Dot A was stressed at an average field of -8.44 MV/CM for 5 seconds, thus causing the flatband voltage to shift from 2 volts to -7.5 volts, indicating that a very high concentration of positive charge had been introduced into the oxide. The capacitor was then subjected to the moderate field of -2.10 MV/cm for 15 minutes, which shifted the flatband voltage to -6.2 volts (this operation is not shown in the Table). The capacitor was subjected to this moderate field for an additional hours, which reduced the flatband voltage to -4.7 volts. Thus a significant

Table 5.1 Typical experimental procedures and the results of photodepopulation on gold-field-plate MAS capacitors in which positive charge storage was induced by high-field stress.

	DOT A	V_{FB}		DOT B	V_{FB}
1.	Fresh Dot	2.0 volts	1.	Fresh Dot	2.05 volts
2.	Negative high field stressing -40 volt, 5 seconds	-7.5 volts	2.	-40 volt stressing, 10 sec.	-7.94 volts
3.	-10 volt stressing, 20 hours	-4.7 volts	3.	-10 volt stressing, 20 hours	-4.0 volts
4.	2.5 eV photodepopulation, 6 hours	-4.3 volts	4.	2.5 eV photodepopulation, 4 hours	-3.77 volts
5.	2.75 eV photodepopulation, 6 hours	-4.0 volts	5.	3.0 eV photodepopulation, 4 hours	-3.7 volts
6.	3.0 eV photodepopulation, 6 hours	-3.65 volts	6.	3.5 eV photodepopulation, 4 hours	-3.18 volts
7.	3.25 eV photodepopulation, 6 hours	-3.55 volts	7.	4.0 eV photodepopulation, 2 hours	-1.35 volts
8.	3.5 eV photodepopulation, 6 hours	-3.05 volts			

amount of positive charge was lost. We believe this to be due to the tunneling of electrons from the silicon substrate into the oxide to recombine with the positive charges located in the vinicity of the interface. The direction of the interface field does not favor this injection; therefore, the reduction of a substantial amount of positive charge indicates that these charges are localized near the interface. After the long-time moderate field stressing, the charge retention ability of the MAS devices was very stable. The MAS structure was then maintained at -2.11 MV/cm and was illuminated by photons with energies ranging from 2.5 eV to 3.5 eV. As can be seen in the Table, the overall result of this was to reduce the flatband voltage from -4.7 V to -3.05 V. The same procedure was performed on Dot B (Table 5.1), with the following results: Negative stress at 8.44 MV/cm caused the flatband voltage to shift from 2.1 volts to -7.9 volts. Following a moderate-field bias at -2.11 MV/cm for 20 hours, the flatband voltage moved to -4 volts, i.e., a large fraction of the positive charge was lost. The sample was then exposed to 2.5 eV, 3.0 eV and 3.5 eV light for 4 hours each to photodepopulate the positive trapped charge. A total flatband change of 0.82 volt was observed after this photobleaching process. However, when the sample was exposed to 4 eV light for 2 hours, we found a flatband shift from -3.19 volts to -1.35 volts, and a strong C-V stretch-out also appeared.

During the negative high-field stressing of the MAS capacitors, electrons were injected into the oxide from the gold field plate by trap-assisted tunneling. The build-up of positive charge within the oxide is therefore accompanied by the capturing of electrons close to the front surface. This makes difficult the task of distinguishing whether the observed flatband shift is due to the depopulation of positive charges or the depopulation of trapped electrons followed by recombination of some of the electrons with the positive charges. However, the photodepopulation result shows most of the positive charges with optical energy levels to be located deeper than 3.5 eV from the Al_2O_3 valence band. The significant amount of flatband voltage reduction found during the 3.7-4.0 eV photobleaching process is probably due to electrons undergoing photoassisted tunneling from the metal field plate into the Al_2O_3, after which some of them recombined with trapped holes.

Although photodepopulation is not effective in causing emission of the positive charges, we have presented observations in a previous report showing that the positive charge can be annealed out at moderate temperatures (e.g., at 300°C for several hours). With the presence of both positive charges and electron traps in the oxide, the electrons injected into the oxide can be either recombined with positive charges or be captured into electron traps. We found in the following experiment that at least part of the positive charge can exist in compensation with trapped electrons within the insulator. Two dots were used for this test. The results are shown in Table 5.2. Dot B was subjected to negative average field of -8.44 MV/cm for 5 seconds. After this high field stressing, the flatband voltage was found to have shifted to -7.6 volts. The sample was then biased at -2.11 MV/cm for two hours, reducing the flatband voltage to -5.75 volts. The illumination of the MAS capacitor by 3.75 eV photons for three hours caused the flatband voltage to shift to -2.75 volts. In our photodepopulation studies presented in the last report,[3] the photodepopulation was found to be a relatively slow process. The rapid reduction of flatband voltage seen here is thus due to the optically assisted injection of electrons from the metal field plate into the oxide and subsequent recombination with the positive charges. Following long-time illumination, the flatband voltage was reduced to -1 volt. The sample was then biased at 1.48 MV/cm and irradiated by 5 eV photons for 80 minutes. The total number of charges injected was about 10^{14} cm^{-2}. After this process, a flatband voltage shift to 8.0 volt was observed as shown in Table 5.2. Photons with energies ranging from 2.5 eV to 4.0 eV were then utilized to photo-depopulate the trapped charge while the sample bias was maintained at -1.47 MV/cm. After the photodepopulation process, the flatband voltage was observed to have shifted to 1.85 volts which is even smaller than the flatband voltage of the fresh dot. Similar results were obtained for Dot A as is shown in Table 5.2.

As was shown in the previous report,[3] when the Al_2O_3 insulator is populated with trapped electrons, it is not possible to depopulate the trapped electrons completely by photobleaching. Some deeply trapped electrons which cannot be removed by photons with energies of 4.0 eV

Table 5.2 Typical experimental procedures and results of photodepopulation on two Au-field-plate MAS capacitors in which positive charge storage was induced by negative high-field stress.

	DOT A	V_{FB}(VOLTS)		DOT B	V_{FB}(VOLTS)
1.	Fresh Dot	2.15	1.	Fresh Dot	2.0
2.	Negative high field stressing -40 volt 15 seconds	-7.5	2.	Negative high field stressing -40 volt 5 seconds	-7.6
3.	-10 volt 4ev illumination 7 hours	-1.75	3.	-10 volt 2 hours	-5.75
4.	+7 volt 5 ev photoinjection 40 minutes	7.85	4.	-10 volt 3.75 ev illumination 7 hours	-1.0
5.	-1.45mv/cm for 20 hours	5.5	5.	+7 volt 5 ev photoinjection 75 minutes	8.0
6.	-1.45mv/cm 3.0 ev photodepopulation 1 hour	4.75	6.	-1.45mv/cm for 15 hours	5.55
7.	-1.45mv/cm 3.25 ev photodepopulation 1 hour	4.5	7.	-1.45mv/cm 2.5 ev photodepopulation 3 hours	5.05
8.	-1.45mv/cm 3.5 ev photodepopulation 1 hour	3.75	8.	-1.45mv/cm 2.75 ev photodepopulation 3 hours	4.6
9.	-1.45mv/cm 3.75 ev photodepopulation 1 hour	3.1	9.	-1.45mv/cm 3.0 ev photodepopulation 3 hours	4.05
10.	-1.45mv/cm 4.0 ev photodepopulation 1 hour	2.6	10.	-1.45mv/cm 3.25 ev photodepopulation 3 hours	3.15
11.	-1.45mv/cm 4.0 ev photodepopulation 1 hour	2.25	11.	-1.45mv/cm 3.5 ev photodepopulation 3 hours	2.4
12.	-1.45mv/cm 3.8 ev photodepopulation 3 hours	2.00	12.	-1.45mv/cm 3.75 ev photodepopulation 3 hours	1.85

still remain in the oxide. Usually, these deeply trapped electrons contributed a flatband voltage of 1-2 volts. Therefore, the positive charges did not recombine with the injected electrons completely. Although most of the trapped holes had been neutralized by injected electrons, some positive charges remained and existed in compensation with trapped electrons. It appears that the electrons injected into the oxide did not necessarily have a better opportunity to recombine with all the positive charges. This suggests that the electron traps are Couloumbic-attractive in nature. Due to the large capture cross section of the electron traps, the finite amount ($10^{14}cm^{-2}$) of injected electrons did not recombine with the positive charges completely. Instead, some of the electrons were trapped and existed in compensation with the remaining positive charges.

5.4 Further Studies of the Al_2O_3 Insulator Strength

(A) Breakdown Field of MAS Capacitors

As was shown in Figs. 4.1(a),(b) in a previous report,[2] the field strength of the Al_2O_3 insulator depends on the length of time that the stress is applied. In order to study the detailed breakdown process in a consistent way, each sample was biased for two hours at a field close to the critical field. If no breakdown occurred, the bias was increased by one volt and held again for two hours. This process was repeated until a breakdown occurred. In a previous report[1] we showed the results for positive field. Here we show the results for negative field. The negative field strengths obtained for capacitors from different wafers are shown in Figs. 5.11 and 5.12. Both p- and n-type substrates were available. The figures show the cumulative percentage of broken-down capacitors vs. gate voltage. The smooth curves are continuous approximations to the discrete data. The field at which 50% of the capacitors had broken down is noted in each curve. Table 5.3 summarizes the values of field so defined for both n- and p-type substrates, both field polarities, aluminum and gold field plates, and two temperatures: 95°K and 300°K. These aluminum-oxide insulators were all grown at 900°C.

The insulator strength is observed to be dependent on the bias polarity. As shown in Table 5.3, the oxide can sustain a larger field when the metal field plate is biased negatively with respect to the

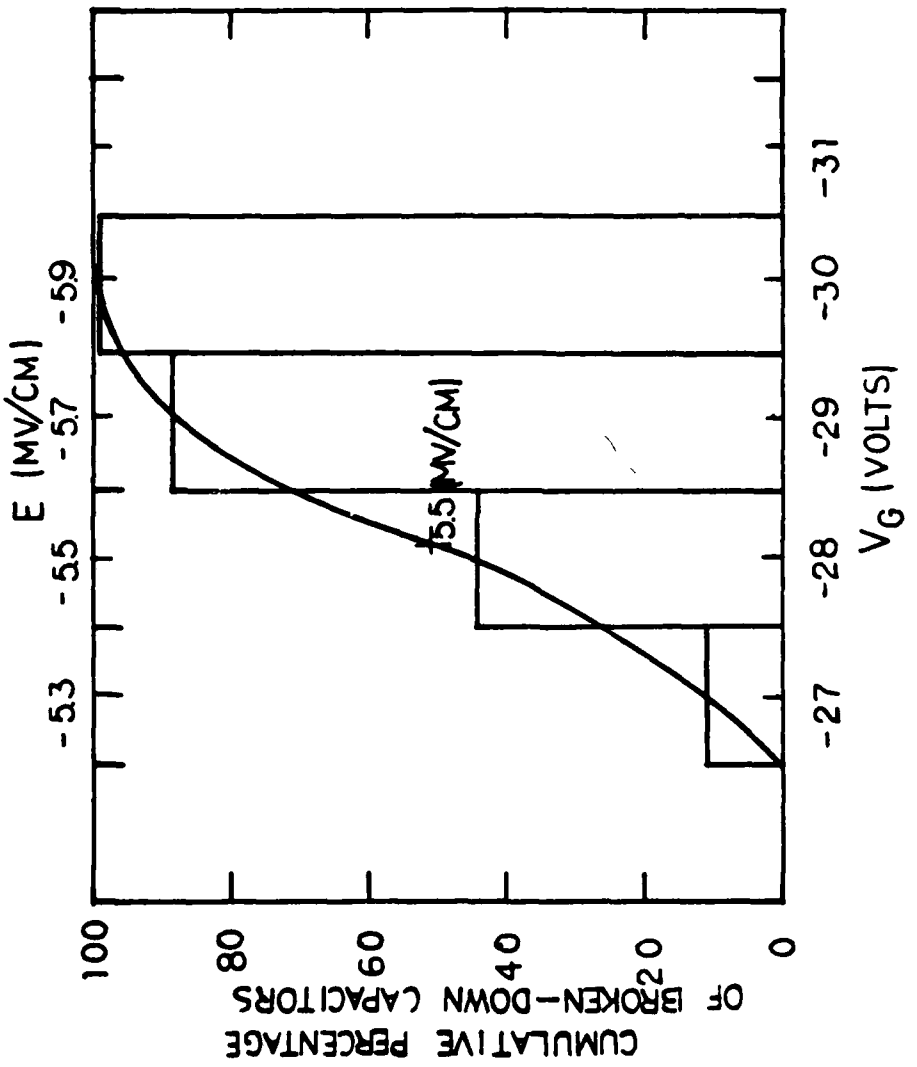

FIG. 5.12. Similar to Fig. 5.11, but for 8 capacitors on a single p-type wafer having gold field plates. Data taken at room temperature. Oxide: 509Å grown at 900°C.

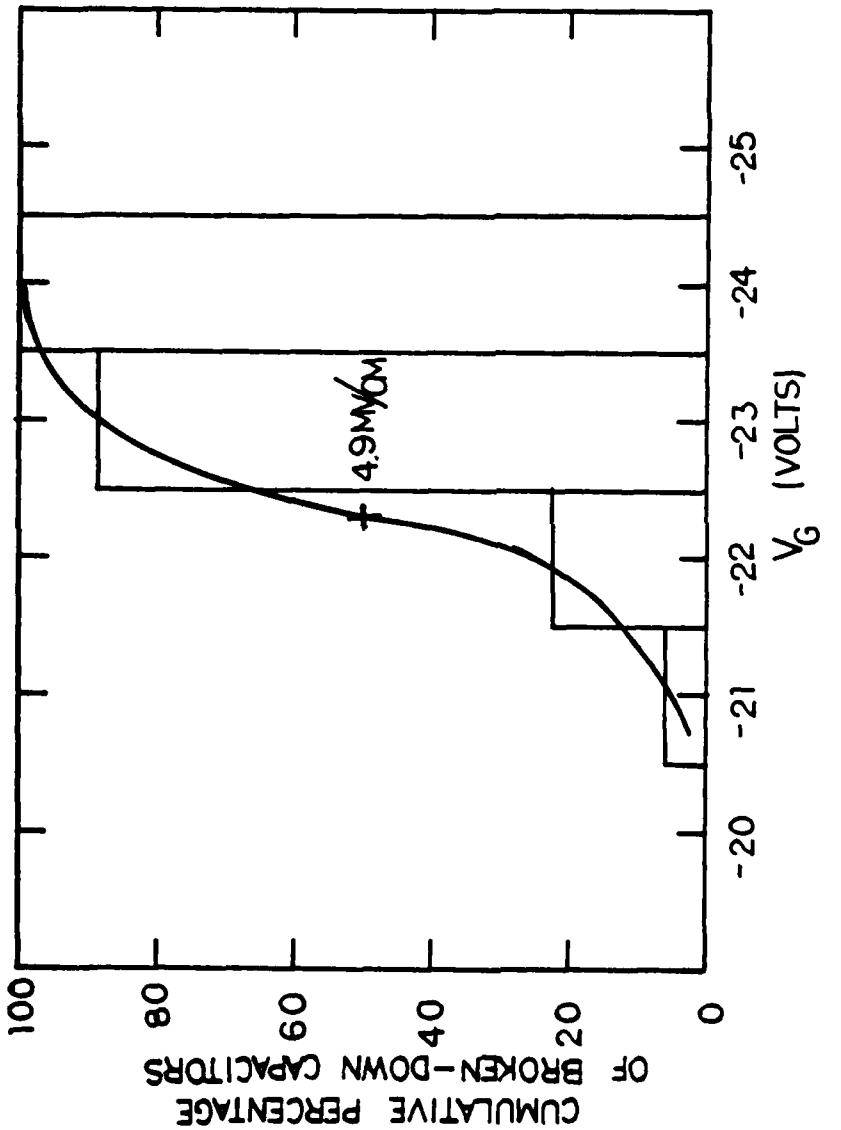

FIG. 5.11. Cumulative percentage of broken-down MAS capacitors vs. applied voltage for 25 capacitors on a single p-type wafer. The field plates were aluminum. The voltage was incremented in 1-volt steps and each step was held for 2 hours at room temperature. The curves are continuous approximations to the discrete data. Oxide: 450Å grown at 900°C.

substrate. Under negative high field stressing, both the current level and the breakdown field are larger than those measured using positive field, as shown in Figs. 1(a),(b) of a previous report.[2] Thus, more heat is generated in the insulator during negative high-field stressing but without breaking down the sample, indicating that the breakdown mechanism is not initiated by a thermal runaway process.[7,8] The samples with gold field plates can withstand even stronger negative fields, as is indicated in Table 5.3. With regard to the improved dielectric strength at liquid nitrogen temperature[1,2] shown in Table 5.3, we take this to be strong evidence against impact ionization as the mechanism initiating breakdown.

(B) Comparison of Insulators Prepared at Different Temperatures

It has been observed by several investigators[9-11] that Al_2O_3 insulating films can be deposited on a heated silicon substrate at temperatures ranging from 400°C to 1000°C. However, the deposited films showed significant differences in etch rates and electron diffraction patterns for deposition temperatures below 700°C and above 800°C. The high-temperature deposited films showed a polycrystalline type of insulator structure, while the low-temperature deposited films were amorphous.[10-12] In our studies, the electronic characteristics and dielectric strengths for two high-temperature-prepared samples were compared, and we show the results as follows: The effect of positive high-field on the high-frequency C-V curves is shown in Fig. 5.13 for Al_2O_3 prepared at 900°C and in Fig. 5.14 for Al_2O_3 prepared at 815°C, both substrates being n-type silicon. The insulator thickness was 450Å for both sets of samples. In both figures, Curve 1 is for the fresh sample. A bias of +7 volts was then applied for 5 minutes, resulting in C-V curves numbered 2 in both figures. This bias was incremented by +2 volts and held for 5 additional minutes, resulting in Curves 3. Further increments of +2 volts, each held for 5 minutes, up to a maximum bias of +17 volts, resulted in Curves 4-7. The samples prepared at 900°C show much more stable C-V characteristics than those prepared at 815°C, and the 815°C samples show C-V stretch-out and hysteresis. On the other hand, as is shown by Fig. 5.15, the currents in the two sets of samples show little difference. We believe that the hysteresis observed in the C-V curves of the 815°C samples is the result of a high concentration of

SAMPLES	BREAKDOWN FIELD STRENGTH			
	+ AT 300°K	− AT 300°K	+ AT 95°K	− AT 95°K
AL/450Å AL_2O_3 N-SI SUB	4.0 MV/CM		5.0 MV/CM	
AL/450Å AL_2O_3 N-SI SUB	4.4 MV/CM			
AL/988Å AL_2O_3 N-SI SUB	4.0 MV/CM			
AL/450Å AL_2O_3 P-SI SUB	4.1 MV/CM	-4.9 MV/CM		-5.9 MV/CM
AU/509Å AL_2O_3 P-SI SUB	~4.0 MV/CM	-5.5 MV/CM		

Table 5.3 The average field strength for samples from five different wafers with different oxide thicknesses and different types of electrode materials. The field strength was measured at two different temperatures: 95°K and 300°K.

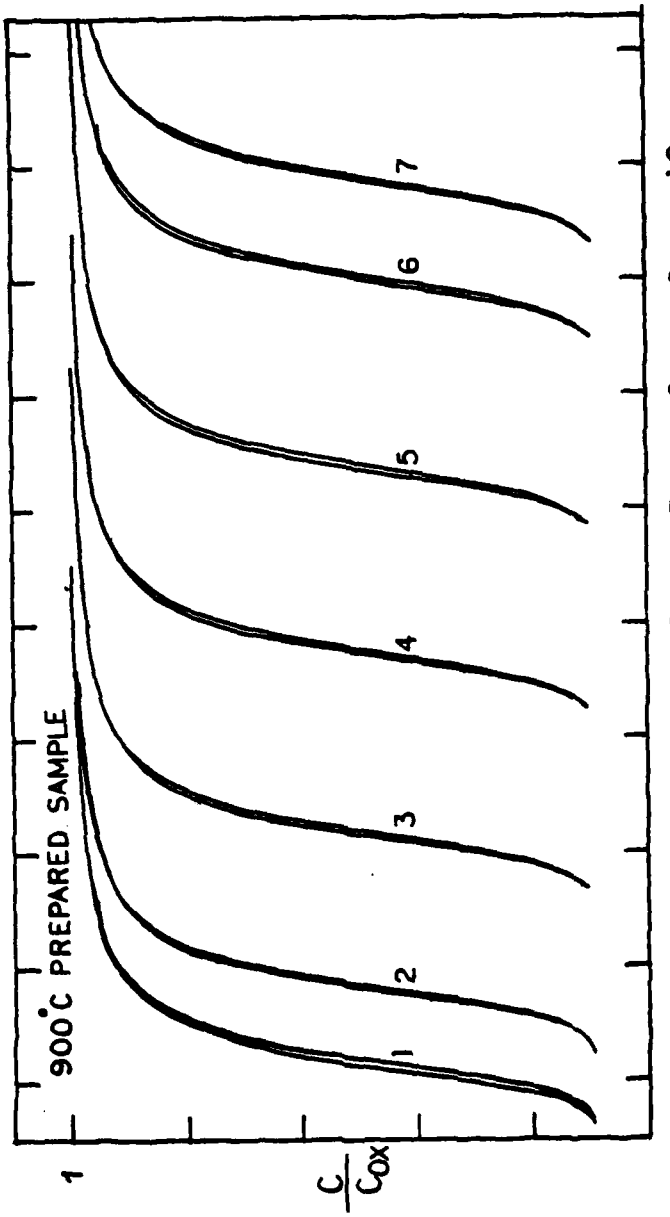

FIG. 5.13. High-frequency C-V curves showing the effect of high-field charging of MAS capacitors prepared at 900°C. Curve 1 is the initial curve. For the remaining curves, voltages ranging from +7 V to +17 volts, with two-volt increments between steps, were applied for 5 minutes each. The insulator thickness was 450Å.

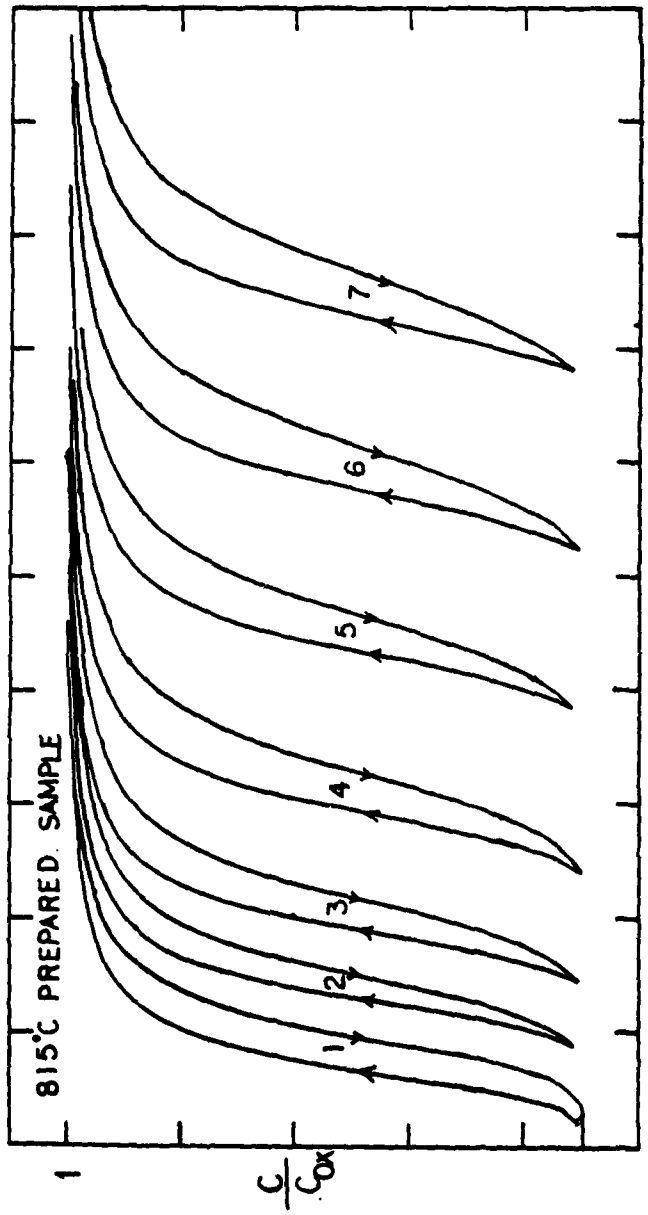

FIG. 5.14. Similar to FIG. 5.12, but for samples prepared at 815°C. The insulator thickness was 450Å.

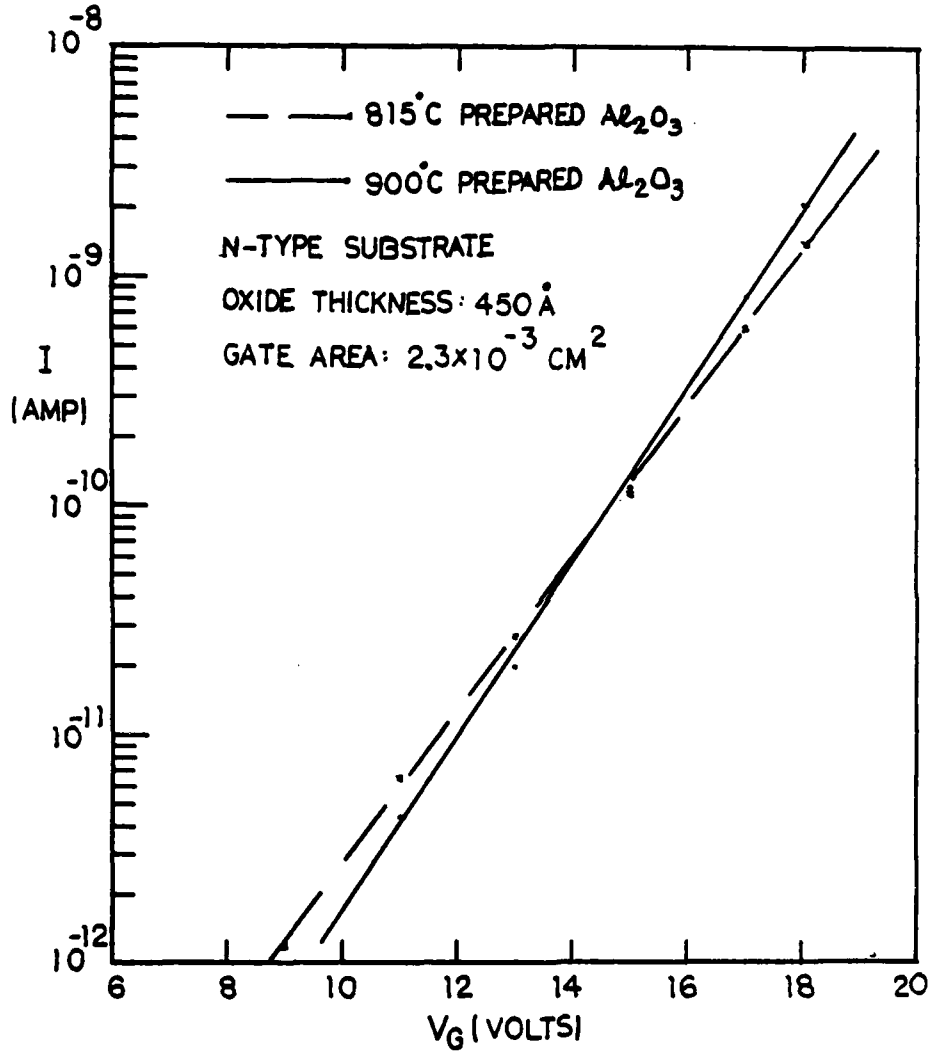

FIG. 5.15. I-V characteristics for samples prepared at 815°C and 900°C. The current was monitored while stressing the capacitors at each voltage for five minutes. The applied voltage ranged from +7 V to +17 V with two-volt increments at each step.

electron traps in the Si-Al_2O_3 interface region which can exchange carriers with the silicon substrate during the C-V measurement.

The breakdown figures given in Table 5.3 were for 900°C oxides. For comparison we tested five capacitors having 815°C oxides. One of the dots broke down after 100 min at 3.56 MV/cm, while four other dots broke down while stressed at 3.8 MV/cm, one after 5 min, the second at 44 min, the third at 50 min, and the fourthat 65 min. As a check, six additional 815°C samples were tested. One dot broke down after 64 min at 3.8 MV/cm, and the other five dots underwent current runaway while stressed at 4.0 MV/cm, the times being 25 min, 30 min, 35 min, 60 min, and 64 min. Comparison of these results with those of Table 5.3 shows that oxides prepared at high temperature can sustain higher fields under positive bias. We found that if the 815°C oxides were annealed at 300°C in vacuum for two hours, the dielectric strength improved significantly. We tested four annealed dots by stressing them at 4 MV/cm for 2 hours. Only one dot underwent current runaway before the end of the run (at 100 minutes). None of the unannealed samples could sustain this field for such a long period.

The foregoing comparisons were on samples with n-type substrates stressed with positive bias. The comparison is extended to negative bias, using p-type substrates, in Figs. 5.16-5.18 for both 815°C and 900°C aluminum oxides. The I-V curves of Fig. 5.16 again show only a small discrepancy between the currents, especially at the higher fields. Comparison of the C-V characteristics of Figs. 5.17 and 5.18 again show that the 815°C oxide exhibits a large hysteresis loop in comparison with the 900°C oxide, and, in addition, the net positive flatband voltage shift was smaller under the same negative stressing conditions. Therefore, the 815°C capacitor seems to have more hole traps located in the vicinity of the interface which can capture holes from the substrate and re-emit them. From the results of the C-V curve measurements on 815°C oxides deposited on both n-type and p-type samples, it would appear that significant amounts of hole traps and electron traps were located near the interface. The presence of these traps is speculated to be the result of the mismatching of ions, resulting in dangling bonds and dislocated ions. For samples prepared at the lower temperatures, the chemical reaction did not go to completion and left a more disturbed area near the interface region.

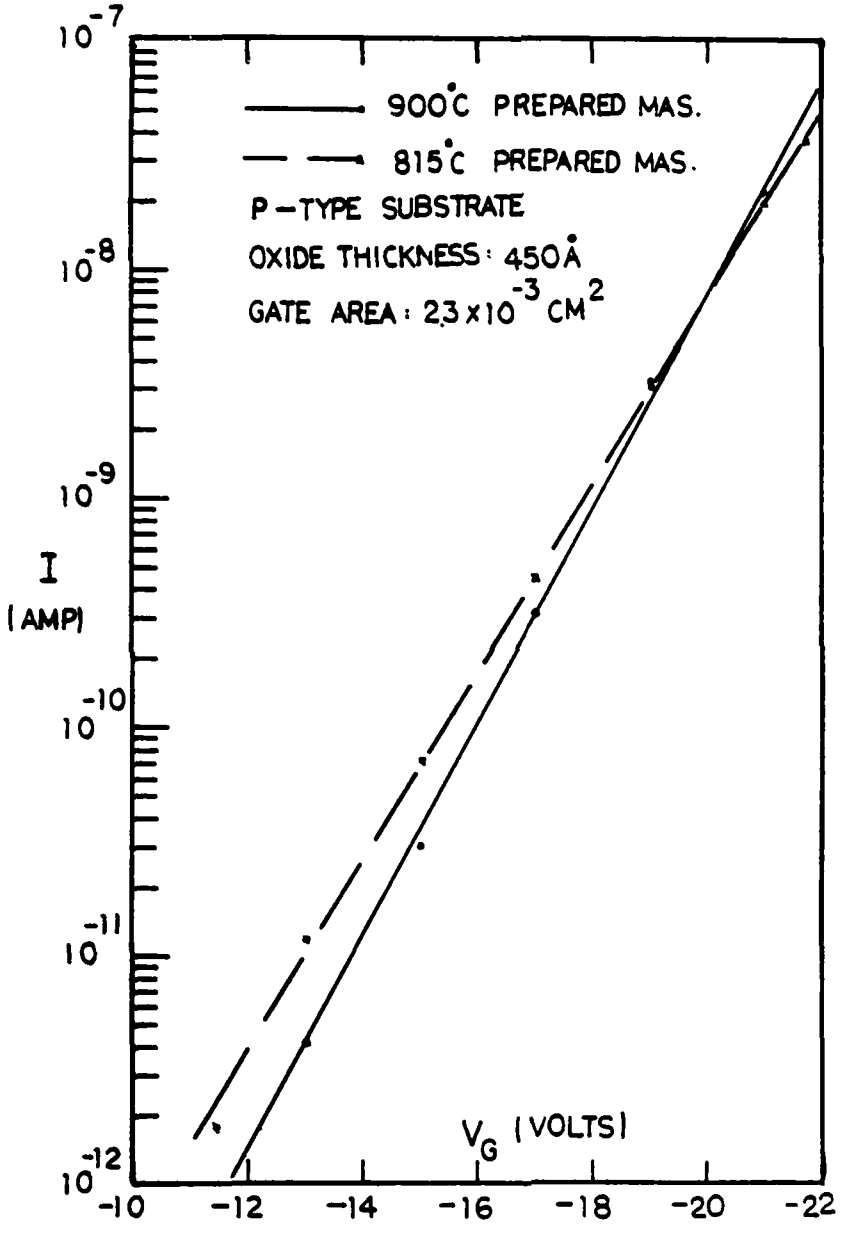

FIG. 5.16 I-V characteristics for p-substrate samples prepared at 815°C and 900°C. The current was monitored while stressing the capacitors at each constant voltage for 5 minuts. The applied voltage ranged from -7 volts to -17 volts with two-volt increments at each step.

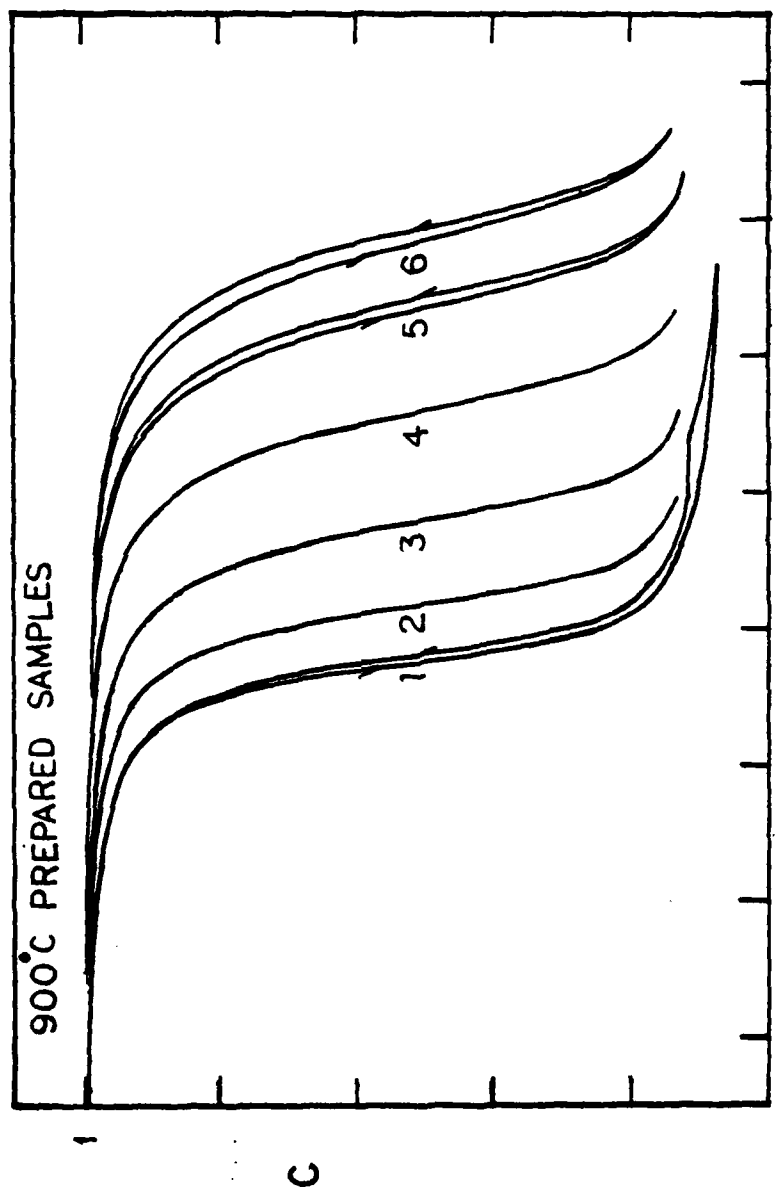

FIG. 5.17. High field charging of the MAS capacitors prepared at 900°C. The C-V curve was measured after stressing the capacitor at each voltage for five minutes. The applied voltage ranged from -7 volts to -17 volts with two-volt increments at each step.

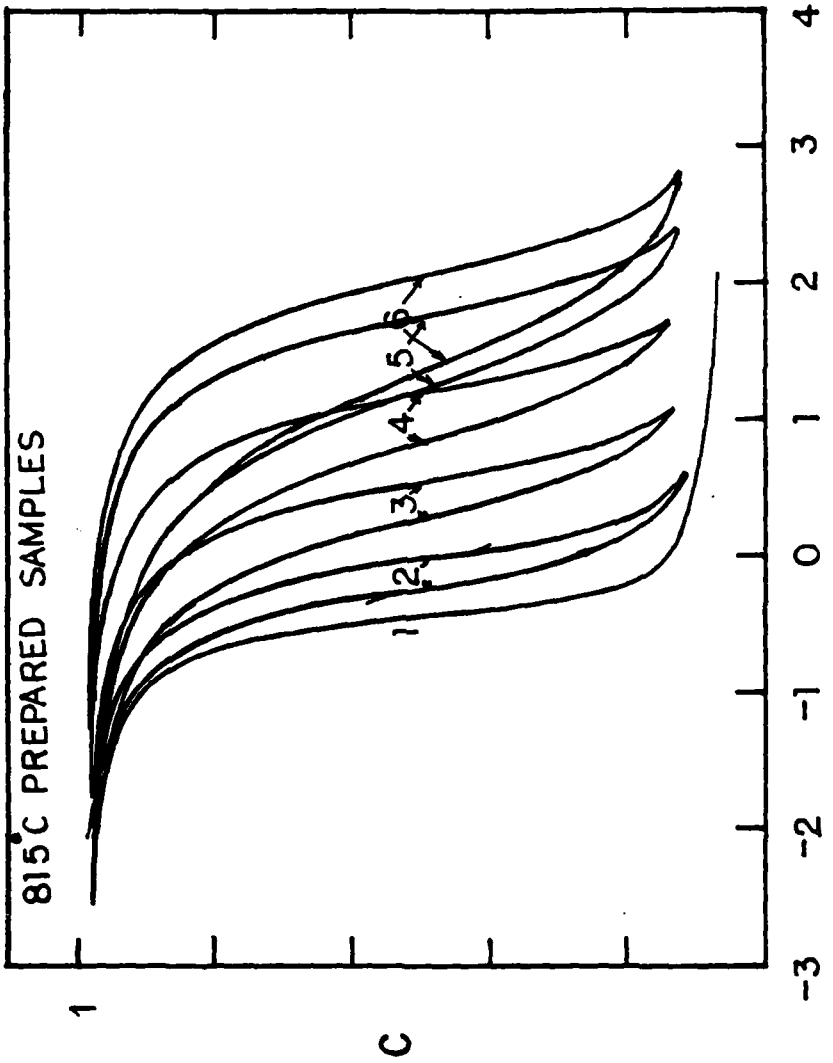

FIG. 5.18. Similar to previous figures, but for samples prepared at 815°C.

The insulator strength under negative field stressing was found to be essentially independent of the deposition temperature. Although the silicon substrate and the Al_2O_3 insulator interface did not seem to match as well for the 815°C oxide, this did not seem to influence the oxide field strength under negative field stressing. The breakdown mechanism under negative field stressing was thus not initiated from the Al_2O_3-Si interface region. Thermal annealing of the p-substrate 815°C samples did not produce an increase in negative-field dielectric strength. An interpretation of these results will be given later.

(C) Negative High Field Stress Followed by Moderate Positive Field Stress

As was shown in Table 5.3, the gold-field-plate MAS capacitors were able to withstand relatively high breakdown fields. During the strong negative field stressing, significant amounts of positive charge were introduced into the oxide. In comparison with the results obtained with positive field stressing, the build-up rate of positive charge is much slower under negative field stress. Three sets of samples having Au field plates were tested. The oxides were all deposited at 900°C. One had an n-type substrate and a 509Å oxide, the second had a p-type substrate and an 881Å oxide, and the third had an n-type substrate and a 1089Å oxide. Following strong negative field stressing (~-6.0MV/cm), significant positive charge appeared in all the oxides, and C-V stretch-out was observed. The MAS capacitors having an oxide thickness of 509Å were then biased at a moderate positive field (3.5 MV/cm). This was observed to cause a very high frequency of self-quenched breakdowns, whereas this breakdown phenomenon was only rarely observed for fresh samples under the same positive field stress. More systematic studies of this phenomenon were conducted on the MAS capacitors having an oxide thickness of 1089Å. As is shown in Table 5.4, following negative field stress of -6.1 or -6.4 MV/cm, application of the more moderate positive stress of +4.4 MV/cm resulted in a high frequency of self-quenched breakdowns. (The number of breakdowns was normalized to an area of 1 mm^2 and a stress time of 60 minutes.) This is to be contrasted with the result obtained when a field of +4.4 MV/cm is applied to a fresh sample, for this produces a normalized frequency of breakdowns between zero and one per mm^2 per 60 min. Thus

	DOT				
	A	B	C	D	E
FIRST (NEGATIVE) STRESS: $\bar{E}$ (MV/CM)	-6.1 →				-6.4
STRESS TIME (MIN)	40	90	90	120	30
NORMALIZED NUMBER OF SQBDs PRODUCED AT $\bar{E}$ = 4.4 MV/CM	22	16	21	8	300
NORMALIZED NUMBER OF SQBDs PRODUCED AT $\bar{E}$ = 4.4 MV/CM AFTER THERMAL ANNEALING	2.0	2.4	12	0	2.0
CONDITIONS OF 120 MIN ANNEAL :					
AMBIENT :	VAC.	VAC.	N_2	VAC	VAC
TEMPERATURE (°C) :	300	300	215	212	212
CONTACTS :	OPEN	OPEN	OPEN	SHORT	OPEN

Table 5.4 Effect of negative high field stressing on the dielectric strength under subsequent positive stress. The number of self-quenched breakdowns is normalized to an area of $1mm^2$ and a time of 60 min. After thermal annealing, the samples were restored almost to their original strength.

the prior application of a negative field weakens the oxide for subsequent positive fields. As is shown in Table 5.4, thermal annealing in vacuum or in N_2 restores the sample strength. Samples A, B and E were annealed in vacuum at 212°C or 300°C with the terminals open circuited. Sample C was annealed in N_2 at 215°C with the terminals open circuited, and sample D was annealed in vacuum at 215°C with the terminals short circuited. Following the annealing, the sample almost recovered its original dielectric strength. Figure 5.19 shows the C-V curves of a typical sample at various stages in the resting. Curve 1 is for the fresh sample. Curve 2 was taken after negative stress at an average field of -6.1 MV/cm, and shows positive trapped charge. Curves 3 and 4 were taken after subsequent positive stress, and show a buildup of trapped electrons. Annealing resulted in Curve 5, and subsequent positive stress resulted in Curve 6.

Our interpretation of the foregoing results is as follows: When a sufficiently large negative voltage is applied to the field plate, either holes are introduced into the oxide from the substrate or electrons are field-emitted from atomic bonds near the interface. In either case the result is a laterally nonuniform positive charge in the oxide, near the Si-Al_2O_3 interface. The positive charge is caused by a lack of electrons in bonding orbitals and is possibly accompanied by a localized displacement of the atoms. The positively charged centers serve as interface states if they are so close to the interface that they can exchange charge readily with the substrate. Positively charged centers somewhat farther from the interface will serve as electron traps. Owing to the noncrystalline nature of the oxide, different positive centers will find themselves in somewhat different surroundings and, electronically, will have different energy levels for trapping. Deep levels will be able to trap electrons stably, while shallow levels can serve to aid electron injection from the substrate when the field plate is made positive. Thus, when the field plate is sufficiently negative, the formation of the positive centers near the Si-Al_2O_3 interface causes the flatband voltage to go negative. The effect is particularly prominent when the field plate is Au rather than Al, for with Al, its smaller work function permits a larger injection of electrons from the negative field plate, and these electrons tend to recombine with the positive centers and annihilate

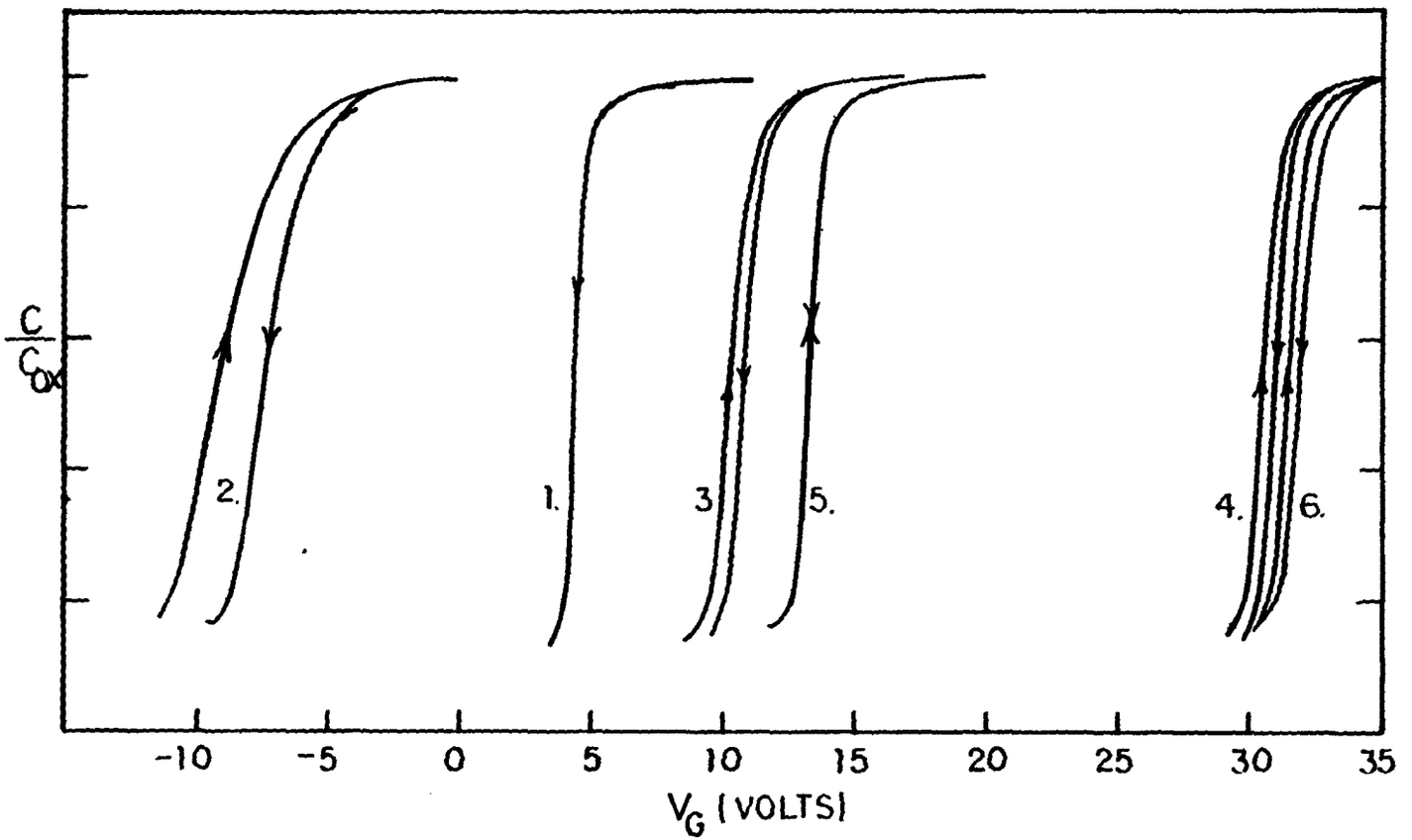

FIG. 5.19. Effect on the C-V curves of negative stress followed by positive stress. The samples were Au-1089Å Al_2O_3-n-silicon substrate MAS capacitors. Curve 1 is the C-V curve for the fresh MAS capacitor. Curve 2 was taken after stressing the capacitor at -66 volts for 60 minutes. Curve 3 was taken after subsequently applying +23 volts for 15 minutes. Curve 4 was taken after stressing at +48 volts for 60 minutes. The sample was then annealed at 300°C in vacuum for 2 hours. Curve 5 was obtained after annealing. Curve 6 was taken after stressing the annealed capacitor at +48 volts for 2 hours.

some of them. If the field plate is now made positive, the shallow positive centers near the Si-Al_2O_3 interface aid the electron injection from the substrate in a laterally nonuniform and localized way, and this leads to localized breakdown at comparatively modest field strengths. The lower breakdown strength of the oxides deposited at 815°C, compared with those deposited at 900°C, can be explained by assuming that the 815°C oxides have a larger density of stressed bonds from which bonding electrons can be field emitted. After the Si-Al_2O_3 interface has been stressed and has acquired localized positive charges, thermal annealing can relax the area and restore the original dielectric strength.

5.5 Summary and Conclusions

We have studied the high-field injection of electrons from the silicon substrate into the Al_2O_3 insulator of MAS capacitors, and find that at sufficiently low temperatures (below ~102°K in our samples), the injected current in independent of temperature but is strongly field dependent. We believe that at these temperatures the injection is by tunneling into nearby defect states in the oxide, with subsequent hopping into states farther from the interface and finally injection into the conduction band of the oxide. The current is limited by the ability of the hopping process to empty the states near the interface so that further tunneling can take place. At higher temperatures the field dependence is not so great and, above about 200°K, an Arrhenius plot shows an activation energy of about 0.35 eV. We believe that at these temperatures the defect states are being emptied thermally into the conduction band of the oxide and that this thermal emission is the limiting factor in the injection.

We have obtained data on the charge storage and charge retention of our aluminum oxides. Back tunneling of electrons trapped near the interface originally produces a fast decrease in the stored charge, but the storage becomes reasonably stable in times of the order of a few minutes.

A finding that is of significance to the high-field strength of the oxide is that a large electric field (4-6 MV/cm) applied with the field plate negative results in the formation of localized centers of

positive charge near the Si-Sl_2O_3 interface. This is in addition to the trapping of injected electrons through the bulk of the oxide. The localized positive centers are especially prominent if a gold field plate is used instead of the usual aluminum, for the higher work function of the gold restricts the injection of electrons from the field plate and thus reduces the amount of trapped negative charge in the oxide. Interface states are formed, apparently connected with the positive charges. Presumably the same effect would be caused with the field plate positive, but here the localized positive centers would be located just under the field plate and could not be observed by C-V measurements. After a large negative field has been applied and we observe the presence of the localized positive charges, the ability of the capacitor to withstand positive fields is impaired. We believe that the reason for this is that the positive centers aid the injection of electrons from the substrate, and they do this in a localized manner, thus leading to easier localized breakdown.

We find that our aluminum oxide samples prepared at 815°C are inferior in breakdown strength to those prepared at 900°C, and we believe this to be due to the greater density of localized states through which electrons can be injected.

We find that the dielectric strength of our aluminum oxides is better at 95°K than at 300°K, confirming our belief that impact ionization is not an important factor in the breakdown. With positive field plate at 300°K, we find an average breakdown strength of about 4.0 MV/cm for either gold or aluminum field plates. The material of the field plate should not matter when the polarity is positive, for the breakdown comes about from electron injection from the substrate. With negative field plate at 300°K, we find an average breakdown field of about 4.9 MV/cm for aluminum field plates and about 5.5 MV/cm for gold field plates. The gold is superior when the field plate is negative, for breakdown comes about from electron injection from the field plate, and gold, with its higher work function, produces less electron injection at a given interface field.

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